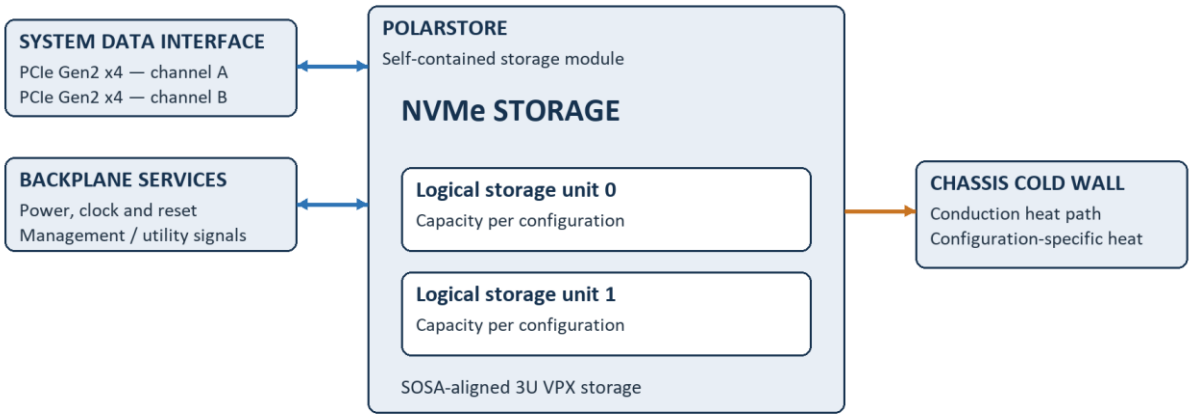
POLAR STORE N-Series 8 TB
ICD & User Guide

CAVU
AEROSPACE

This manual defines the common external interfaces, installation, operation and storage configuration of the SOSA-aligned PolarStore N-series family. It combines the interface control document, external RAID guidance, integration procedure and pin reference in one customer document.



Two equal logical units. Capacity and power follow the ordered configuration.

Characteristic	Specification
Storage organisation	Two equal logical units; capacity by configuration
Data interface	Two PCIe Gen2 x4 channels on P2
Power / heat	Configuration-specific; see the order configuration record
Board dimensions	100 x 160 mm; conduction-cooled 3U VPX
System independence	Generic PCIe system connection; no prescribed companion OBC

Capacity is selected by configuration. The 8 TB-class configuration provides two equal 4 TB-class logical units: 7.68 TB nominal per card and 3.84 TB per unit before formatting and RAID metadata.

Contents

Units and identity

TB is decimal capacity (10^12 bytes). Capacity-class labels follow the ordered configuration; the 8 TB example has two 4 TB-class logical units. Logical-unit identifiers remain distinct from PCIe channel names and operating-system discovery order. Register unit identity against the module serial number when configuring external storage.

Document control

Revision 0.5 establishes one N-series family document set. Capacity examples are separate from the common interface. Power, heat and mass are defined for each ordered configuration. The pin signal and direction inventory is retained from the preceding revision.

The ICD & User Guide and standalone Pin Assignment use the same position inventory. The colour reference presents the same signals by wafer with columns i through a.

1. Product and system interface

PolarStore is a family of self-contained NVMe storage modules with two equal logical storage units. A compatible system PCIe initiator/root complex accesses the module through the backplane. No particular processor card, OBC family or storage-management product is prescribed.

Interface	Customer function
P0 utility	Supply, reference clocks, reset and system utility
P1	Reserved high-speed data positions; defined utility discretes
P2 data	Channel A: W1-W4; channel B: W5-W8
P2 utility	Clock, reset and management functions at W13-W16; reserved functions as listed
Cooling	Conduction through card guides to chassis cold wall
External storage policy	Independent units or optional external RAID

1.1 Storage organisation

Capacity is selected by configuration. The 8 TB-class configuration provides two equal 4 TB-class logical units: 7.68 TB nominal per card and 3.84 TB per unit before formatting and RAID metadata.

Two modules in the two-unit configuration provide four logical storage units. Unit labels identify resources available to system software; the delivery presentation record supplies stable identifiers, block format and access-path mapping.

1.2 System responsibilities

The system provides backplane power, the selected clock/reset services, compatible PCIe routing and software access. Optional RAID, array monitoring, backup, scrub and rebuild belong to the external storage-management system. Section 7 covers these functions.

1.3 Applicability

This document covers the PolarStore N-series, SOSA-aligned 3U VPX NVMe storage family using the P0/P1/P2 interface defined here. Capacity options share this reference when they use the same connector allocation and electrical interface revision. The order configuration identifies capacity, mass, power, thermal limits and fitted keying.

1.4 Family configuration selection

This document covers the PolarStore N-series, SOSA-aligned 3U VPX NVMe storage family using the P0/P1/P2 interface defined here. Capacity options share this reference when they use the same connector allocation and electrical interface revision. The order configuration identifies capacity, mass, power, thermal limits and fitted keying.

Configuration field	Family definition
Product family	PolarStore N-series; NVMe storage only
Common interface	Two PCIe Gen2 x4 channels; the connector map in this manual
Capacity selection	Total nominal capacity and capacity class are specified on the order
Logical organisation	Two equal logical storage units; each provides half the card nominal capacity
Assembly mass	Specified per configuration, including retention hardware
Power and heat	Separate idle, active and transient limits for the ordered configuration
Keying	Key 1 = 315 degrees; Key 2 follows the target-slot schedule

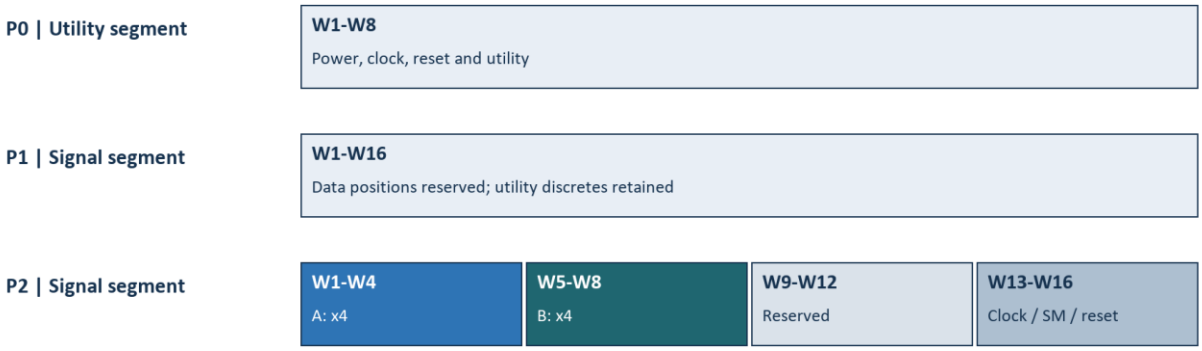
Capacity example — 8 TB class

Card class	Logical-unit class	Nominal card / unit capacity
8 TB	2 x 4 TB	7.68 TB / 3.84 TB

Other ordered capacities use the same documents when the external interface revision is unchanged. Capacity class is a product label; nominal bytes and formatted usable capacity are distinct. RAID capacity is calculated separately.

The configuration record accompanies the module order and identifies its numerical mass, idle and active input power, transient current, heat dissipation and thermal boundary conditions. Values from one capacity configuration are not applied to another.

2. Connector and backplane routing



Connector allocation. P2 carries both x4 data links; P1 retains utility discretes.

SOSA-aligned 3U payload storage. Backplane routing: P0 utility; P1 data positions reserved; P2 channel A at W1-W4 and channel B at W5-W8. Match the full power, utility and signal allocation when selecting the slot and backplane.

Region	Function	Routing requirement
P0 W1-W8	Power, clock and utility	Match rail, return and utility coordinates
P1 W1-W16	Utility discretes; data reserved	Route assigned utilities; reserved data undriven
P2 W1-W4	PCIe channel A x4	Four TX pairs and four RX pairs
P2 W5-W8	PCIe channel B x4	Four TX pairs and four RX pairs
P2 W9-W12	Data reserved	Observe individual row-i functions
P2 W13-W16	Clocks, reset and management	Match the selected utility interface

Connect system TX to storage RX and storage TX to system RX. Preserve lane index and differential polarity; select system port coordinates from that system interface. Both required x4 routes terminate at the storage slot. Appendix A lists every lane pair and pin.

The storage routing and utility allocation define backplane compatibility. The SOSA profile of a different processing or storage module does not substitute for this connector map. Physical keying and mating orientation follow the module/backplane drawings.

3. Power and heat dissipation

Supply	Nominal value	Connector allocation
VS1	12 V	P0 W1.f/g/h and W2.f/g/h
Auxiliary	3.3 V	P0 W5.e
VBAT	Per electrical interface	P0 W3.i
VS2 / VS3	No module connection	Do not connect an alternative supply

3.1 Operating states

State / quantity	Definition for the ordered configuration
Idle input power	Whole-card power with no user I/O, after entry to the configured low-power state
Active input power	Whole-card read/write power under the specified workload and temperature
Activity limit	At most two storage drives active concurrently per card; applies across all logical units
Peak / inrush	Separate amplitude and duration for startup, wake-up and supply transients
Heat dissipation	Steady card input power is the chassis heat-load basis; use the configuration thermal limit

The activity limit also applies during RAID rebuild, scrub, background maintenance and transitions. Non-active storage follows the configured power policy. A logical unit is not a count of simultaneously active physical drives.

3.2 Power and thermal sizing

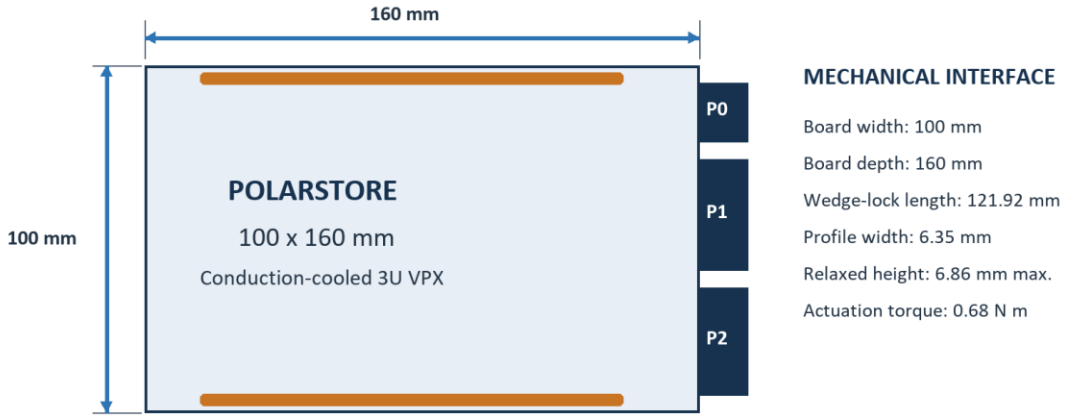
Use the ordered configuration's numerical idle, active, transient and thermal limits. Idle power does not size the active cooling requirement. Sum the applicable loads for multiple cards and add the system margin; capacity alone is not a power-scaling rule.

Provide a continuous conduction path through the retainers and card guides to the chassis cold wall. Use the configuration card-edge temperature and mounting conditions; do not assume equal heat flow through both edges.

3.3 Supply sequencing

Apply the electrical interface limits for voltage tolerance, ripple, inrush, per-rail current, protection and sequencing. Total power divided by 12 V is not a per-rail current limit. Section 8 covers installation and first power.

4. Mechanical interface



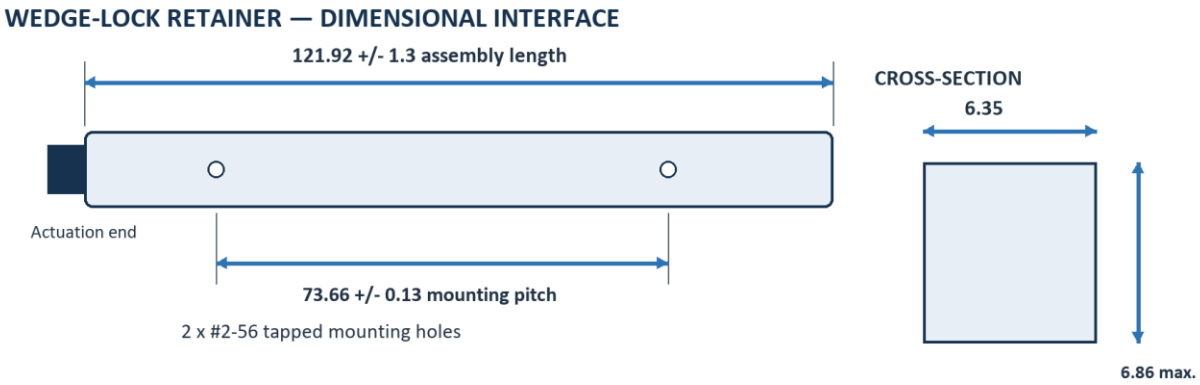
All dimensions in mm. Connector blocks and retainer locations identify interface regions; use assembly datums for mating.

Parameter	Specification
Board dimensions	100 mm width x 160 mm depth
Format	3U VPX, single slot, conduction cooled
Retention	Screw-actuated wedge-lock retainers
Retainer envelope	121.92 mm length x 6.35 mm width; 6.86 mm maximum relaxed height
Assembly mass	Configuration-specific; supplied with delivery data
Installed pitch and envelope	As specified by the delivered mechanical drawing
Mating / keying	P0/P1/P2 module segments; match chassis connector and key positions

The drawing above identifies the board dimensions and external interface regions. Connector projection, assembly thickness, insertion access and exact retainer locations follow the module assembly drawing. Use the chassis and module datums when checking fit and engagement.

Retainers provide mechanical clamping and thermal contact. Their 121.92 mm body length is distinct from the 160 mm board depth. The recommended guide gap is also distinct from the slot-to-slot pitch.

4.1 Wedge-lock dimensions and actuation



3/32 in (2.38 mm) hex drive | Tightening torque: 0.68 N m (6 lbf in)

Recommended chassis gap: retained assembly thickness + 7.62 mm. The gap is not the VPX slot pitch.

Retainer dimensions apply to the selected 4.80 in length. Mounting position on the card follows the assembly drawing.

Retainer parameter	Dimension / requirement
Assembly length	121.92 mm (4.80 in), tolerance +/- 1.3 mm
Profile width	6.35 mm (0.250 in)
Maximum relaxed height	6.86 mm (0.270 in)
Mounting holes	Two #2-56 tapped holes
Mounting-hole pitch	73.66 mm, tolerance +/- 0.13 mm
Hex drive	3/32 in (2.38 mm)
Actuation torque	0.68 N m (6 lbf in)
Recommended chassis guide gap	Retained board/module assembly thickness + 7.62 mm

Release the retainers before insertion or extraction. After the module is fully seated, tighten each retainer to the actuation torque with a calibrated tool. The actuation torque applies to the wedge-lock screw, not the separate mounting fasteners. Use the assembly procedure for mounting-fastener torque.

Source: nVent SCHROFF Series 260 Card-Lok dimensional and installation data. The values above apply to the selected length and standard screw configuration. Full supplier traceability is maintained outside the customer part description.

5. Clocks, reset and management

Function	Storage allocation	Role
Primary REF_CLK +/-	P0 W8.g / h	100 MHz clock input allocation
AUX_CLK +/-	P0 W8.c / d	Additional clock positions
REF_CLK_A / B +/-	P2 W13.e/f; W14.g/h	Alternative reference positions; source selection required
AUX_CLK_A / B +/-	P2 W13.a/b; W14.c/d	Additional clock positions
SYSRESET*	P0 W4.c	Storage reset input
SYSRESET_A* / B*	P2 W13.i; W15.i	Additional reset input allocations
SM_RESET_A* / B*	P1 W9.i; W11.i	Management reset inputs
SP_FAIL_A* / B*	P1 W3.i; W13.i	Fault output allocations
SM / geographic address	P0 and P2; see pin tables	Management bus and slot-address signals
NVMRO	P0 W4.b	Write-protection control input allocation

5.1 Electrical ownership and sequencing

IN/OUT refer to the storage card. * denotes active-low naming; it does not specify output drive type. The electrical schedule defines logic levels, pull-ups, power-off tolerance, default states and which clock/reset positions are used. Do not drive all allocated clock inputs simultaneously without a defined source-selection contract.

Hold the storage interface in reset until the selected rails and clock meet their stability limits. The timing schedule specifies reset drive/pulse width, supply-to-reset and clock-to-reset delays, link training, enumeration and recovery timeouts. Clock format, jitter/SSC, coupling and termination must match the complete channel design.

5.2 Management and reserved signals

The management schedule defines SM bus pairing, protocol, addresses, commands, telemetry units and fault latch/clear behaviour. Four SM signal positions are not four independent buses. NED means Nuclear Event Detector; NED and NED_RETURN are reserved. SPI positions are reserved with no command service. JTAG and NVMRO electrical and access rules use the configuration schedule.

6. Storage service and performance

Two equal logical storage units; capacity follows the ordered configuration.

Capacity is selected by configuration. The 8 TB-class configuration provides two equal 4 TB-class logical units: 7.68 TB nominal per card and 3.84 TB per unit before formatting and RAID metadata.

Each logical unit is separately addressable. Logical units share the card failure domain. The delivered presentation record defines actual unit identifiers, block format, addressable block counts and host access paths.

Storage interface item	Integration definition
Unit count / nominal capacity	2 equal units; each is half the ordered nominal card capacity
Unit identity	Stable identifier associated with parent card serial number
Host discovery	Delivered PCI identity, driver/OS compatibility and controller/function presentation
NVMe, where selected	Controller/namespace IDs, supported commands, queues and error behaviour
Channel-to-unit mapping	Defined by delivery interface; no fixed mapping inferred from unit count
Write durability	Completion, caching and flush/FUA semantics in the persistence contract

6.1 Bandwidth

Gen2 uses 5 GT/s per lane. After 8b/10b encoding, one x4 link has a 2 GB/s ceiling per direction before transaction overhead. Two independent x4 paths have a 4 GB/s combined ceiling; a shared x4 switch upstream limits their combined traffic to 2 GB/s before other traffic and overhead. These values are interface encoding limits; use the delivered workload performance for application sizing.

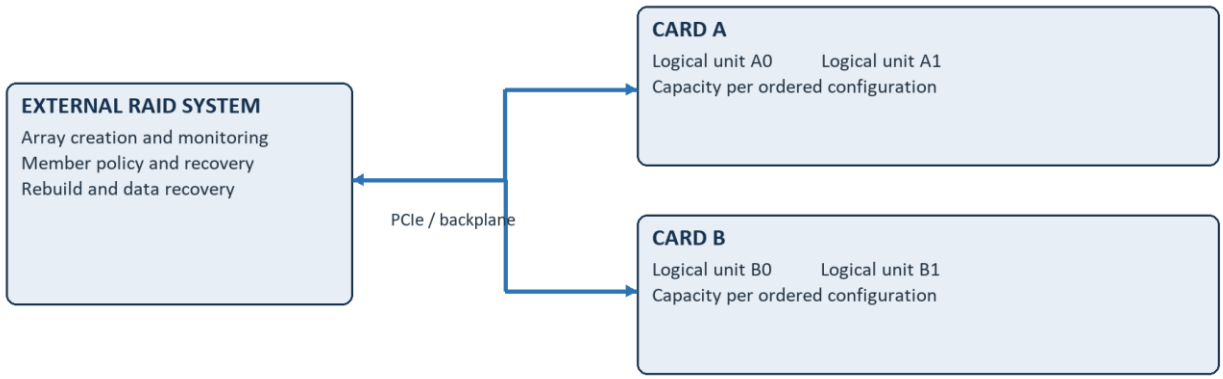
Sustained read/write throughput, random IOPS and latency are reported against the delivered workload, transfer size, queue depth, system route and thermal condition. Use the performance record for the applicable module and system configuration.

7. External RAID and storage organisation

Numerical examples in this section use the 8 TB-class configuration (7.68 TB nominal per card). For another capacity, substitute the ordered nominal capacity; RAID method and member placement are unchanged.

8 TB class per card | Dual 4 TB-class logical units | External system RAID

Each card provides an 8 TB-class storage resource that can be organised as two equal 4 TB-class logical units. Two cards provide four units. The nominal capacity is 3.84 TB per unit, 7.68 TB per card, before formatting. This guide covers optional external RAID; a card can also be used with its units independently.



Cross-card mirror pairs: A0 + B0 and A1 + B1. Two cards provide four logical storage units.

7.1 Ownership and discovery

The external host or compatible system RAID controller creates and manages the array. Array metadata, member placement, failure policy, rebuild, scrubbing and recovery belong to that external system. Compatibility and the supported RAID levels depend on the selected RAID implementation and delivered storage presentation.

A0/A1 and B0/B1 in this guide are example logical labels. Record actual stable unit identifiers and parent card serial numbers; operating-system device order can change after reset or replacement. Controller and namespace identifiers are recorded in the delivery storage interface.

A pair of logical units on one card shares that card failure domain. Splitting capacity does not create two independent cards.

7.2 RAID capacity and member placement

Numerical examples in this section use the 8 TB-class configuration (7.68 TB nominal per card). For another capacity, substitute the ordered nominal capacity; RAID method and member placement are unchanged.

Cards / units	Host arrangement	Nominal usable capacity
1 card / 2 units	Independent units	7.68 TB
1 card / 2 units	RAID 0	7.68 TB
1 card / 2 units	RAID 1	3.84 TB
2 cards / 4 units	Independent units	15.36 TB
2 cards / 4 units	Two cross-card RAID 1 arrays	7.68 TB total
2 cards / 4 units	RAID 10	7.68 TB

Capacities assume equal 3.84 TB members. RAID and filesystem metadata, formatting and configured reserves reduce available user space. One TB is 10^12 bytes. The product capacity class must not be interpreted as 8.00 TB of addressable space.

7.2.1 One card

Independent mode exposes two separate 3.84 TB resources. RAID 0 combines their capacity to 7.68 TB with no redundancy. RAID 1 stores mirrored data and yields 3.84 TB. A single-card mirror can remain usable only if a failure leaves another member accessible and intact; it cannot protect against card loss or common faults affecting both units.

7.2.2 Two cards

Independent mode exposes A0, A1, B0 and B1, each 3.84 TB. For two cross-card mirrors, pair A0 with B0 and A1 with B1. Each mirror yields 3.84 TB; together they yield 7.68 TB. RAID 10 stripes across these two mirror pairs to yield 7.68 TB in one array, subject to host support.

To tolerate loss of either card, place one member of every mirror on each card. Pairing A0 with A1 and B0 with B1 cannot provide that protection for RAID 10: losing a card removes both members of a mirror.

7.2.3 More than two cards

For N equal-capacity cards of nominal capacity C TB, independent storage provides 2N logical units and N x C TB before overhead. Two-way mirroring provides N x C / 2 TB when every unit has an equal partner. Define the actual failure tolerance from member placement; the card count alone does not establish it.

7.3 RAID configuration and recovery

Numerical examples in this section use the 8 TB-class configuration (7.68 TB nominal per card). For another capacity, substitute the ordered nominal capacity; RAID method and member placement are unchanged.

Step	External host / system action
1. Discover	Verify each card and both units; record stable identifiers, block format and actual capacity
2. Place members	Associate every unit with its parent card; choose independent, stripe or mirror policy
3. Create array	Use the supported external RAID tool; verify selected members before any destructive operation
4. Record	Save level, member IDs, mirror pairing, stripe size, metadata version and configuration backup
5. Validate	Write/read verification data; check full capacity, restart behaviour and agreed fault responses
6. Operate	Monitor health and array state; apply the defined flush, backup and shutdown policies

7.3.1 Rebuild and replacement

Replace only after the host has identified the failed card or unit and the array state. A replacement member must have a compatible format and at least the required addressable capacity; a matching marketing capacity label is insufficient. Confirm the replacement identity before clearing metadata or starting rebuild.

The host manages rebuild order, rate and completion checks. Loss of one card can remove two members at once. Verify that the selected RAID implementation supports that failure pattern and that each required mirror retains a good member. Rebuild time and I/O impact depend on workload, routing, policy and errors.

7.3.2 Acceptance scenarios

Test independent access to every unit, stable discovery after restart, the selected array capacity, degraded operation, replacement/rebuild, interrupted rebuild and recovery after controlled reset or power loss. Card-loss testing means testing loss of both units on that card under controlled conditions; it does not imply live removal is supported.

For a two-card cross-card mirror arrangement, verify operation with either card unavailable and verify data after recovery. Host, backplane, power and software availability remain system dependencies. RAID does not protect against every software error, corruption or accidental deletion; the system backup policy remains separate.

8. Installation and first power

PolarStore | SOSA-aligned system integration

8.1 Establish the delivered configuration

With chassis power removed, release the wedge-locks, align the module to its keyed slot and seat the connectors using the prescribed insertion mechanism. Tighten the wedge-lock actuation screws to 0.68 N m. Do not use retainer tightening to draw an unseated connector into engagement. Confirm cooling contact before applying power.

Record storage card serial/revision and software, system interface and software, backplane route, chassis, connector and approved interface schedules. Use sections 1-6 for the external contract and Appendix A for coordinate definitions. Physical integration uses the approved configuration-specific pin map and electrical schedule.

Check	Required outcome before power-on
Mechanical fit	Correct slot/keying, mating orientation, envelope, retention and cooling contact
Power and returns	Correct rail positions/polarity; limits, inrush and protection settings approved
PCIe routing	Each system TX reaches storage RX; lane/polarity preserved; both required system ports reach the slot
Clock and reset	Selected source, termination, logic levels, ownership and sequencing defined
Utility / reserved pins	Management pairing and address defined; reserved pins undriven

8.2 First power and discovery

Apply the approved power and reset sequence with current and voltage monitoring. Record inrush, steady operation, reset release and link-training results against the electrical schedule. Stop and investigate an out-of-limit condition before continuing.

Confirm host enumeration using the delivered driver and discovery record. In the two-unit configuration, identify two equal units per card. Record actual block counts, unit identifiers, parent card serial numbers and host access paths. Verify that discovery after restart preserves identity even if device order changes.

Use dedicated test units or protected test areas for write verification. Array creation, formatting and recovery operations can erase existing data; the operator must identify the intended units and preserve required data before proceeding.

8.3 Integration and acceptance

Test	Evidence and pass criterion
Capacity / identity	Two units per card; equal capacity per agreed block count; stable unique IDs
Data path	Write/read checksums on every unit; no unexplained mismatch or command failure
Performance	Results at agreed request sizes, queue depths and thermal condition meet contracted limits
External RAID	Selected level and members match the configuration record; usable capacity matches calculation
Fault / degraded mode	Affected units correctly identified; selected policy preserves or fails access as specified
Rebuild / replacement	Correct new member selected; rebuild completes and data verifies
Reset / power cycle	Identity and array state recover; persistence follows the agreed durability contract
Thermal / power	Measured values remain within the approved configuration limits throughout workload

8.3.1 Two-card verification

For four independent units, verify access to all four. For cross-card mirrors, prove that each mirror spans cards. Test loss of card A and card B separately under controlled conditions and verify the expected degraded state. Do not substitute loss of a single logical unit for a complete card-loss test.

8.3.2 Acceptance record

Record test ID, configuration/serial numbers, tool versions, setup, limits, observations, pass/fail, anomalies and retained logs. Missing limits or unexecuted scenarios remain untested; they are not passes. Environmental and assurance testing follows the contracted programme.

At handover provide the signed configuration record, approved interface schedules, measured acceptance results, unit/member mapping, external RAID configuration backup and recovery instructions. Document verification alone does not establish hardware acceptance.

9. Data integrity and lifecycle

9.1 Persistence contract

The delivered host/storage contract shall define when a completed write is durable, the scope of volatile caching, flush and FUA behaviour where supported, and the treatment of commands interrupted by power loss or reset. RAID does not replace this persistence contract or a backup policy.

For controlled shutdown, stop new application writes, complete outstanding I/O, synchronise the filesystem and external array, issue the supported storage flush operation, check completion and then remove power according to the electrical schedule. The system shall not assume arbitrary power-loss protection or hot insertion/removal from this interface.

9.2 Fault reporting and recovery

Event	Required integration behaviour to verify
Logical-unit I/O error	Report the affected stable unit identity and error; external RAID handles member policy
Card or PCIe path loss	Identify all inaccessible units; do not confuse path loss with independent media failures
Reset during I/O	Resolve outstanding commands and re-establish identity before mounting or reassembling arrays
Power interruption	Recover consistently to the agreed durability boundary; report incomplete work
Member replacement	Verify new identity and capacity before host-controlled rebuild; prevent stale-member reuse

10. Delivery configuration and support

Retain the module serial number and revision, software release, electrical interface record, mechanical drawing and acceptance report with the system configuration. These records establish the values and procedures applicable to the installed equipment.

Record	System integration use
Module identification	Serial number, hardware revision and software release
Mechanical interface	Assembly envelope, pitch, mass, datums, keying and retention details
Electrical interface	Supply limits, inrush, timing, utility levels and clock selection
Storage presentation	Stable unit IDs, capacity, block format, access-path mapping and driver versions
External array configuration	RAID implementation, member IDs, mirror placement and recovery settings
Acceptance results	Data integrity, performance, thermal and lifecycle results for the installed configuration

Service and replacement

Record symptoms, affected card/unit identities, array state and retained logs before requesting support. Before replacing equipment, follow the external system recovery and data-preservation procedure. Reconfirm replacement capacity, block format and identity before permitting rebuild.

Document set

Appendix A contains the complete pin assignment and lane routes. The standalone Pin Assignment reproduces the same data. The single HTML Connector Reference provides colour-coded wafer tables, expandable pin details, terminology and keying.

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Appendix A — Pin assignment

PolarStore | SOSA-aligned storage | Revision 0.5

This document covers the PolarStore N-series, SOSA-aligned 3U VPX NVMe storage family using the P0/P1/P2 interface defined here. Capacity options share this reference when they use the same connector allocation and electrical interface revision. The order configuration identifies capacity, mass, power, thermal limits and fitted keying.

A.0 Connector coordinates

P0/P1/P2 identify module connector segments; J0/J1/J2 identify mating backplane segments. P2.W1.a identifies P2, wafer 1, row a. The detailed list follows wafer order with rows a through i. The colour reference displays columns i through a; the position labels remain identical.

Segment	Logical positions	Storage interface
P0	72 (8 wafers x 9 rows)	Supply, reset, utility and reference clocks
P1	144 (16 x 9)	Reserved data positions; utility discretes
P2	144 (16 x 9)	Two PCIe x4 channels and utility functions

The 360-position reference includes key gaps and backplane-only returns. It is a coordinate inventory; a key gap is not a contact and a backplane-only return is not a module pad.

Code	Meaning
IN / OUT / I/O	Input / output / bidirectional relative to the storage card
PWR / GND	Supply / module return
RES / NC	Reserved: leave undriven / no module connection
BP / --	Backplane-only return / no-contact gap
*	Active-low signal naming

The single HTML connector reference presents the same pin inventory in colour-coded wafer tables with expandable details.

A.1 Lane routes and backplane connection

SOSA-aligned 3U payload storage. Backplane routing: P0 utility; P1 data positions reserved; P2 channel A at W1-W4 and channel B at W5-W8. Match the full power, utility and signal allocation when selecting the slot and backplane.

Channel / lane	Storage TX +/-	Connect to	Storage RX +/-	Connect from
A/0	W1.e/f	System A RX0	W1.a/b	System A TX0
A/1	W2.g/h	System A RX1	W2.c/d	System A TX1
A/2	W3.e/f	System A RX2	W3.a/b	System A TX2
A/3	W4.g/h	System A RX3	W4.c/d	System A TX3
B/0	W5.e/f	System B RX0	W5.a/b	System B TX0
B/1	W6.g/h	System B RX1	W6.c/d	System B TX1
B/2	W7.e/f	System B RX2	W7.a/b	System B TX2
B/3	W8.g/h	System B RX3	W8.c/d	System B TX3

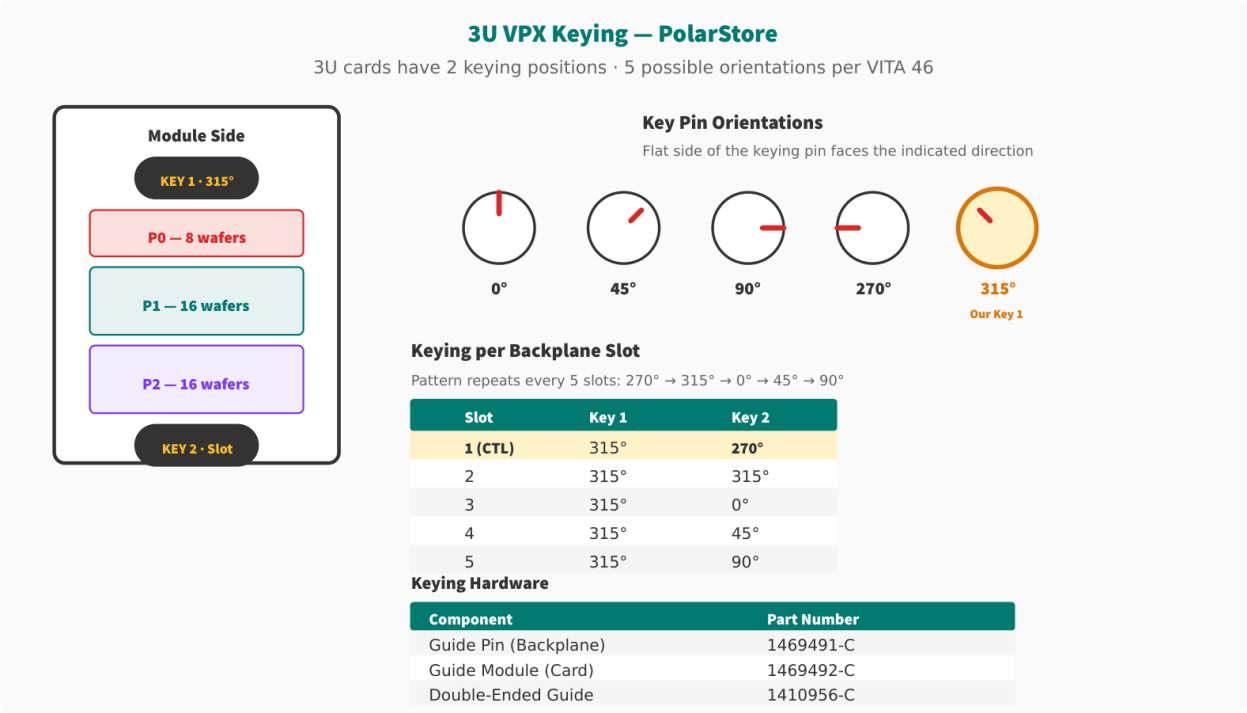
Connection rules

- Connect each storage transmitter to the corresponding system receiver, and each storage receiver to the system transmitter.
- Preserve lane index and differential polarity. Select the system-side port coordinates from that system interface.
- Route both x4 channels to the storage slot. Each channel uses four transmit pairs and four receive pairs.
- Leave reserved signals undriven. Apply the documented clock, reset, management and power connections.
- Match the physical keying and mating orientation before insertion; do not infer orientation from a text-table layout.

Signal-integrity limits, supply tolerances, clock selection and utility electrical levels follow the delivered electrical interface record. Wedge-lock installation and power-on procedures are in the ICD & User Guide.

A.2 Keying guide

Key 1 = 315 degrees for VS1 +12 V. Key 2 is selected by the backplane slot. The module guide must match the target slot.



The slot-key pattern repeats every five slots: 270, 315, 0, 45 and 90 degrees. Slot 1 is the controller reference position. The same convention applies to the PolarStore module guide for its assigned slot.

Suggested suffix: -Kn, where n is the slot number. The capacity configuration and slot-key suffix are separate identifiers. Key orientation is set during assembly and is not field-adjustable.

Match the module and backplane keys before insertion. P0.W1.e, P0.W2.e and P0.W3.e are non-contact gaps in the coordinate map and have no routed electrical connection.

A.3 P0 | Wafers 1-4

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P0.W1.a	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W1.b	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W1.c	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W1.d	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W1.e	No Pad	--	Key gap	Key gap; no contact
P0.W1.f	VS1	PWR	Supply	12 V nominal; see electrical interface
P0.W1.g	VS1	PWR	Supply	12 V nominal; see electrical interface
P0.W1.h	VS1	PWR	Supply	12 V nominal; see electrical interface
P0.W1.i	GDiscrete1	RES	Discrete reserved	Do not drive
P0.W2.a	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W2.b	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W2.c	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W2.d	NC (VS2)	NC	Unused rail	No module connection allocated
P0.W2.e	No Pad	--	Key gap	Key gap; no contact
P0.W2.f	VS1	PWR	Supply	12 V nominal; see electrical interface
P0.W2.g	VS1	PWR	Supply	12 V nominal; see electrical interface
P0.W2.h	VS1	PWR	Supply	12 V nominal; see electrical interface
P0.W2.i	GND	GND	Return	Module signal return
P0.W3.a	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.b	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.c	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.d	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.e	No Pad	--	Key gap	Key gap; no contact
P0.W3.f	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.g	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.h	NC (VS3)	NC	Unused rail	No module connection allocated
P0.W3.i	VBAT	PWR	Supply	Battery role: electrical interface
P0.W4.a	GND	GND	Return	Module signal return
P0.W4.b	NVMRO	IN	Control	Behaviour: electrical interface
P0.W4.c	SYSRESET*	IN	Control	Behaviour: electrical interface
P0.W4.d	NED	RES	NED reserved	Reserved; do not drive
P0.W4.e	NED	RES	NED reserved	Reserved; do not drive
P0.W4.f	GND	GND	Return	Module signal return
P0.W4.g	SM3	I/O	Mgmt	Bus pairing: interface schedule
P0.W4.h	SM2	I/O	Mgmt	Bus pairing: interface schedule
P0.W4.i	GND	GND	Return	Module signal return

A.4 P0 | Wafers 5-8

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P0.W5.a	GND	GND	Return	Module signal return
P0.W5.b	SM1	I/O	Mgmt	Bus pairing: interface schedule
P0.W5.c	SM0	I/O	Mgmt	Bus pairing: interface schedule
P0.W5.d	GND	GND	Return	Module signal return
P0.W5.e	3V3_AUX	PWR	Supply	3.3 V nominal; see electrical interface
P0.W5.f	GND	GND	Return	Module signal return
P0.W5.g	GA4*	IN	Address	Address decode: interface schedule
P0.W5.h	GAP*	IN	Address	Address decode: interface schedule
P0.W5.i	SYS_CON*	IN	Control	Behaviour: electrical interface
P0.W6.a	GND	GND	Return	Module signal return
P0.W6.b	GA0*	IN	Address	Address decode: interface schedule
P0.W6.c	GA1*	IN	Address	Address decode: interface schedule
P0.W6.d	NED_RETURN	RES	NED reserved	Reserved; do not drive
P0.W6.e	NED_RETURN	RES	NED reserved	Reserved; do not drive
P0.W6.f	GND	GND	Return	Module signal return
P0.W6.g	GA2*	IN	Address	Address decode: interface schedule
P0.W6.h	GA3*	IN	Address	Address decode: interface schedule
P0.W6.i	GND	GND	Return	Module signal return
P0.W7.a	TRSTB	IN	JTAG	Levels/rate: electrical interface
P0.W7.b	TMS	IN	JTAG	Levels/rate: electrical interface
P0.W7.c	GND	GND	Return	Module signal return
P0.W7.d	GND	GND	Return	Module signal return
P0.W7.e	TDI	IN	JTAG	Levels/rate: electrical interface
P0.W7.f	TDO	OUT	JTAG	Levels/rate: electrical interface
P0.W7.g	GND	GND	Return	Module signal return
P0.W7.h	GND	GND	Return	Module signal return
P0.W7.i	TCK	IN	JTAG	Levels/rate: electrical interface
P0.W8.a	GND	GND	Return	Module signal return
P0.W8.b	GND	GND	Return	Module signal return
P0.W8.c	AUX_CLK_P	IN	Clock	Source/receiver: electrical interface
P0.W8.d	AUX_CLK_N	IN	Clock	Source/receiver: electrical interface
P0.W8.e	GND	GND	Return	Module signal return
P0.W8.f	GND	GND	Return	Module signal return
P0.W8.g	REF_CLK_P	IN	Clock	Source/receiver: electrical interface
P0.W8.h	REF_CLK_N	IN	Clock	Source/receiver: electrical interface
P0.W8.i	GND	GND	Return	Module signal return

A.5 P1 | Wafers 1-4

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P1.W1.a	RESERVED	RES	Reserved	No data service allocated
P1.W1.b	RESERVED	RES	Reserved	No data service allocated
P1.W1.c	GND-J1	BP	BP return	Backplane-only position
P1.W1.d	GND	GND	Return	Module signal return
P1.W1.e	RESERVED	RES	Reserved	No data service allocated
P1.W1.f	RESERVED	RES	Reserved	No data service allocated
P1.W1.g	GND-J1	BP	BP return	Backplane-only position
P1.W1.h	GND	GND	Return	Module signal return
P1.W1.i	GDiscrete1	RES	Discrete reserved	Do not drive
P1.W2.a	GND	GND	Return	Module signal return
P1.W2.b	GND-J1	BP	BP return	Backplane-only position
P1.W2.c	RESERVED	RES	Reserved	No data service allocated
P1.W2.d	RESERVED	RES	Reserved	No data service allocated
P1.W2.e	GND	GND	Return	Module signal return
P1.W2.f	GND-J1	BP	BP return	Backplane-only position
P1.W2.g	RESERVED	RES	Reserved	No data service allocated
P1.W2.h	RESERVED	RES	Reserved	No data service allocated
P1.W2.i	GND	GND	Return	Module signal return
P1.W3.a	RESERVED	RES	Reserved	No data service allocated
P1.W3.b	RESERVED	RES	Reserved	No data service allocated
P1.W3.c	GND-J1	BP	BP return	Backplane-only position
P1.W3.d	GND	GND	Return	Module signal return
P1.W3.e	RESERVED	RES	Reserved	No data service allocated
P1.W3.f	RESERVED	RES	Reserved	No data service allocated
P1.W3.g	GND-J1	BP	BP return	Backplane-only position
P1.W3.h	GND	GND	Return	Module signal return
P1.W3.i	SP_FAIL_A*	OUT	Fault	Drive/timing: electrical interface
P1.W4.a	GND	GND	Return	Module signal return
P1.W4.b	GND-J1	BP	BP return	Backplane-only position
P1.W4.c	RESERVED	RES	Reserved	No data service allocated
P1.W4.d	RESERVED	RES	Reserved	No data service allocated
P1.W4.e	GND	GND	Return	Module signal return
P1.W4.f	GND-J1	BP	BP return	Backplane-only position
P1.W4.g	RESERVED	RES	Reserved	No data service allocated
P1.W4.h	RESERVED	RES	Reserved	No data service allocated
P1.W4.i	GND	GND	Return	Module signal return

A.6 P1 | Wafers 5-8

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P1.W5.a	RESERVED	RES	Reserved	No data service allocated
P1.W5.b	RESERVED	RES	Reserved	No data service allocated
P1.W5.c	GND-J1	BP	BP return	Backplane-only position
P1.W5.d	GND	GND	Return	Module signal return
P1.W5.e	RESERVED	RES	Reserved	No data service allocated
P1.W5.f	RESERVED	RES	Reserved	No data service allocated
P1.W5.g	GND-J1	BP	BP return	Backplane-only position
P1.W5.h	GND	GND	Return	Module signal return
P1.W5.i	SYS_CON*	IN	Control	Behaviour: electrical interface
P1.W6.a	GND	GND	Return	Module signal return
P1.W6.b	GND-J1	BP	BP return	Backplane-only position
P1.W6.c	RESERVED	RES	Reserved	No data service allocated
P1.W6.d	RESERVED	RES	Reserved	No data service allocated
P1.W6.e	GND	GND	Return	Module signal return
P1.W6.f	GND-J1	BP	BP return	Backplane-only position
P1.W6.g	RESERVED	RES	Reserved	No data service allocated
P1.W6.h	RESERVED	RES	Reserved	No data service allocated
P1.W6.i	GND	GND	Return	Module signal return
P1.W7.a	RESERVED	RES	Reserved	No data service allocated
P1.W7.b	RESERVED	RES	Reserved	No data service allocated
P1.W7.c	GND-J1	BP	BP return	Backplane-only position
P1.W7.d	GND	GND	Return	Module signal return
P1.W7.e	RESERVED	RES	Reserved	No data service allocated
P1.W7.f	RESERVED	RES	Reserved	No data service allocated
P1.W7.g	GND-J1	BP	BP return	Backplane-only position
P1.W7.h	GND	GND	Return	Module signal return
P1.W7.i	SYS_CONP*	IN	Control	Behaviour: electrical interface
P1.W8.a	GND	GND	Return	Module signal return
P1.W8.b	GND-J1	BP	BP return	Backplane-only position
P1.W8.c	RESERVED	RES	Reserved	No data service allocated
P1.W8.d	RESERVED	RES	Reserved	No data service allocated
P1.W8.e	GND	GND	Return	Module signal return
P1.W8.f	GND-J1	BP	BP return	Backplane-only position
P1.W8.g	RESERVED	RES	Reserved	No data service allocated
P1.W8.h	RESERVED	RES	Reserved	No data service allocated
P1.W8.i	GND	GND	Return	Module signal return

A.7 P1 | Wafers 9-12

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P1.W9.a	RESERVED	RES	Reserved	No data service allocated
P1.W9.b	RESERVED	RES	Reserved	No data service allocated
P1.W9.c	GND-J1	BP	BP return	Backplane-only position
P1.W9.d	GND	GND	Return	Module signal return
P1.W9.e	RESERVED	RES	Reserved	No data service allocated
P1.W9.f	RESERVED	RES	Reserved	No data service allocated
P1.W9.g	GND-J1	BP	BP return	Backplane-only position
P1.W9.h	GND	GND	Return	Module signal return
P1.W9.i	SM_RESET_A*	IN	Control	Behaviour: electrical interface
P1.W10.a	GND	GND	Return	Module signal return
P1.W10.b	GND-J1	BP	BP return	Backplane-only position
P1.W10.c	RESERVED	RES	Reserved	No data service allocated
P1.W10.d	RESERVED	RES	Reserved	No data service allocated
P1.W10.e	GND	GND	Return	Module signal return
P1.W10.f	GND-J1	BP	BP return	Backplane-only position
P1.W10.g	RESERVED	RES	Reserved	No data service allocated
P1.W10.h	RESERVED	RES	Reserved	No data service allocated
P1.W10.i	GND	GND	Return	Module signal return
P1.W11.a	RESERVED	RES	Reserved	No data service allocated
P1.W11.b	RESERVED	RES	Reserved	No data service allocated
P1.W11.c	GND-J1	BP	BP return	Backplane-only position
P1.W11.d	GND	GND	Return	Module signal return
P1.W11.e	RESERVED	RES	Reserved	No data service allocated
P1.W11.f	RESERVED	RES	Reserved	No data service allocated
P1.W11.g	GND-J1	BP	BP return	Backplane-only position
P1.W11.h	GND	GND	Return	Module signal return
P1.W11.i	SM_RESET_B*	IN	Control	Behaviour: electrical interface
P1.W12.a	GND	GND	Return	Module signal return
P1.W12.b	GND-J1	BP	BP return	Backplane-only position
P1.W12.c	RESERVED	RES	Reserved	No data service allocated
P1.W12.d	RESERVED	RES	Reserved	No data service allocated
P1.W12.e	GND	GND	Return	Module signal return
P1.W12.f	GND-J1	BP	BP return	Backplane-only position
P1.W12.g	RESERVED	RES	Reserved	No data service allocated
P1.W12.h	RESERVED	RES	Reserved	No data service allocated
P1.W12.i	GND	GND	Return	Module signal return

A.8 P1 | Wafers 13-16

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P1.W13.a	RESERVED	RES	Reserved	No data service allocated
P1.W13.b	RESERVED	RES	Reserved	No data service allocated
P1.W13.c	GND-J1	BP	BP return	Backplane-only position
P1.W13.d	GND	GND	Return	Module signal return
P1.W13.e	RESERVED	RES	Reserved	No data service allocated
P1.W13.f	RESERVED	RES	Reserved	No data service allocated
P1.W13.g	GND-J1	BP	BP return	Backplane-only position
P1.W13.h	GND	GND	Return	Module signal return
P1.W13.i	SP_FAIL_B*	OUT	Fault	Drive/timing: electrical interface
P1.W14.a	GND	GND	Return	Module signal return
P1.W14.b	GND-J1	BP	BP return	Backplane-only position
P1.W14.c	RESERVED	RES	Reserved	No data service allocated
P1.W14.d	RESERVED	RES	Reserved	No data service allocated
P1.W14.e	GND	GND	Return	Module signal return
P1.W14.f	GND-J1	BP	BP return	Backplane-only position
P1.W14.g	RESERVED	RES	Reserved	No data service allocated
P1.W14.h	RESERVED	RES	Reserved	No data service allocated
P1.W14.i	GND	GND	Return	Module signal return
P1.W15.a	RESERVED	RES	Reserved	No data service allocated
P1.W15.b	RESERVED	RES	Reserved	No data service allocated
P1.W15.c	GND-J1	BP	BP return	Backplane-only position
P1.W15.d	GND	GND	Return	Module signal return
P1.W15.e	RESERVED	RES	Reserved	No data service allocated
P1.W15.f	RESERVED	RES	Reserved	No data service allocated
P1.W15.g	GND-J1	BP	BP return	Backplane-only position
P1.W15.h	GND	GND	Return	Module signal return
P1.W15.i	MaskableReset*	IN	Control	Behaviour: electrical interface
P1.W16.a	GND	GND	Return	Module signal return
P1.W16.b	GND-J1	BP	BP return	Backplane-only position
P1.W16.c	RESERVED	RES	Reserved	No data service allocated
P1.W16.d	RESERVED	RES	Reserved	No data service allocated
P1.W16.e	GND	GND	Return	Module signal return
P1.W16.f	GND-J1	BP	BP return	Backplane-only position
P1.W16.g	RESERVED	RES	Reserved	No data service allocated
P1.W16.h	RESERVED	RES	Reserved	No data service allocated
P1.W16.i	GND	GND	Return	Module signal return

A.9 P2 | Wafers 1-4

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P2.W1.a	HOST_A_RX0_P	IN	PCIe	Channel A, lane 0
P2.W1.b	HOST_A_RX0_N	IN	PCIe	Channel A, lane 0
P2.W1.c	GND-J2	BP	BP return	Backplane-only position
P2.W1.d	GND	GND	Return	Module signal return
P2.W1.e	HOST_A_TX0_P	OUT	PCIe	Channel A, lane 0
P2.W1.f	HOST_A_TX0_N	OUT	PCIe	Channel A, lane 0
P2.W1.g	GND-J2	BP	BP return	Backplane-only position
P2.W1.h	GND	GND	Return	Module signal return
P2.W1.i	SPI0_SCK	RES	SPI reserved	Reserved; no command service
P2.W2.a	GND	GND	Return	Module signal return
P2.W2.b	GND-J2	BP	BP return	Backplane-only position
P2.W2.c	HOST_A_RX1_P	IN	PCIe	Channel A, lane 1
P2.W2.d	HOST_A_RX1_N	IN	PCIe	Channel A, lane 1
P2.W2.e	GND	GND	Return	Module signal return
P2.W2.f	GND-J2	BP	BP return	Backplane-only position
P2.W2.g	HOST_A_TX1_P	OUT	PCIe	Channel A, lane 1
P2.W2.h	HOST_A_TX1_N	OUT	PCIe	Channel A, lane 1
P2.W2.i	GND	GND	Return	Module signal return
P2.W3.a	HOST_A_RX2_P	IN	PCIe	Channel A, lane 2
P2.W3.b	HOST_A_RX2_N	IN	PCIe	Channel A, lane 2
P2.W3.c	GND-J2	BP	BP return	Backplane-only position
P2.W3.d	GND	GND	Return	Module signal return
P2.W3.e	HOST_A_TX2_P	OUT	PCIe	Channel A, lane 2
P2.W3.f	HOST_A_TX2_N	OUT	PCIe	Channel A, lane 2
P2.W3.g	GND-J2	BP	BP return	Backplane-only position
P2.W3.h	GND	GND	Return	Module signal return
P2.W3.i	SPI0_SDI	RES	SPI reserved	Reserved; no command service
P2.W4.a	GND	GND	Return	Module signal return
P2.W4.b	GND-J2	BP	BP return	Backplane-only position
P2.W4.c	HOST_A_RX3_P	IN	PCIe	Channel A, lane 3
P2.W4.d	HOST_A_RX3_N	IN	PCIe	Channel A, lane 3
P2.W4.e	GND	GND	Return	Module signal return
P2.W4.f	GND-J2	BP	BP return	Backplane-only position
P2.W4.g	HOST_A_TX3_P	OUT	PCIe	Channel A, lane 3
P2.W4.h	HOST_A_TX3_N	OUT	PCIe	Channel A, lane 3
P2.W4.i	GND	GND	Return	Module signal return

A.10 P2 | Wafers 5-8

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P2.W5.a	HOST_B_RX0_P	IN	PCIe	Channel B, lane 0
P2.W5.b	HOST_B_RX0_N	IN	PCIe	Channel B, lane 0
P2.W5.c	GND-J2	BP	BP return	Backplane-only position
P2.W5.d	GND	GND	Return	Module signal return
P2.W5.e	HOST_B_TX0_P	OUT	PCIe	Channel B, lane 0
P2.W5.f	HOST_B_TX0_N	OUT	PCIe	Channel B, lane 0
P2.W5.g	GND-J2	BP	BP return	Backplane-only position
P2.W5.h	GND	GND	Return	Module signal return
P2.W5.i	SPI0_SDO	RES	SPI reserved	Reserved; no command service
P2.W6.a	GND	GND	Return	Module signal return
P2.W6.b	GND-J2	BP	BP return	Backplane-only position
P2.W6.c	HOST_B_RX1_P	IN	PCIe	Channel B, lane 1
P2.W6.d	HOST_B_RX1_N	IN	PCIe	Channel B, lane 1
P2.W6.e	GND	GND	Return	Module signal return
P2.W6.f	GND-J2	BP	BP return	Backplane-only position
P2.W6.g	HOST_B_TX1_P	OUT	PCIe	Channel B, lane 1
P2.W6.h	HOST_B_TX1_N	OUT	PCIe	Channel B, lane 1
P2.W6.i	GND	GND	Return	Module signal return
P2.W7.a	HOST_B_RX2_P	IN	PCIe	Channel B, lane 2
P2.W7.b	HOST_B_RX2_N	IN	PCIe	Channel B, lane 2
P2.W7.c	GND-J2	BP	BP return	Backplane-only position
P2.W7.d	GND	GND	Return	Module signal return
P2.W7.e	HOST_B_TX2_P	OUT	PCIe	Channel B, lane 2
P2.W7.f	HOST_B_TX2_N	OUT	PCIe	Channel B, lane 2
P2.W7.g	GND-J2	BP	BP return	Backplane-only position
P2.W7.h	GND	GND	Return	Module signal return
P2.W7.i	SPI0_CS0*	RES	SPI reserved	Reserved; no command service
P2.W8.a	GND	GND	Return	Module signal return
P2.W8.b	GND-J2	BP	BP return	Backplane-only position
P2.W8.c	HOST_B_RX3_P	IN	PCIe	Channel B, lane 3
P2.W8.d	HOST_B_RX3_N	IN	PCIe	Channel B, lane 3
P2.W8.e	GND	GND	Return	Module signal return
P2.W8.f	GND-J2	BP	BP return	Backplane-only position
P2.W8.g	HOST_B_TX3_P	OUT	PCIe	Channel B, lane 3
P2.W8.h	HOST_B_TX3_N	OUT	PCIe	Channel B, lane 3
P2.W8.i	GND	GND	Return	Module signal return

A.11 P2 | Wafers 9-12

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P2.W9.a	RESERVED	RES	Reserved	No data service allocated
P2.W9.b	RESERVED	RES	Reserved	No data service allocated
P2.W9.c	GND-J2	BP	BP return	Backplane-only position
P2.W9.d	GND	GND	Return	Module signal return
P2.W9.e	RESERVED	RES	Reserved	No data service allocated
P2.W9.f	RESERVED	RES	Reserved	No data service allocated
P2.W9.g	GND-J2	BP	BP return	Backplane-only position
P2.W9.h	GND	GND	Return	Module signal return
P2.W9.i	SPI0_CS1*	RES	SPI reserved	Reserved; no command service
P2.W10.a	GND	GND	Return	Module signal return
P2.W10.b	GND-J2	BP	BP return	Backplane-only position
P2.W10.c	RESERVED	RES	Reserved	No data service allocated
P2.W10.d	RESERVED	RES	Reserved	No data service allocated
P2.W10.e	GND	GND	Return	Module signal return
P2.W10.f	GND-J2	BP	BP return	Backplane-only position
P2.W10.g	RESERVED	RES	Reserved	No data service allocated
P2.W10.h	RESERVED	RES	Reserved	No data service allocated
P2.W10.i	GND	GND	Return	Module signal return
P2.W11.a	RESERVED	RES	Reserved	No data service allocated
P2.W11.b	RESERVED	RES	Reserved	No data service allocated
P2.W11.c	GND-J2	BP	BP return	Backplane-only position
P2.W11.d	GND	GND	Return	Module signal return
P2.W11.e	RESERVED	RES	Reserved	No data service allocated
P2.W11.f	RESERVED	RES	Reserved	No data service allocated
P2.W11.g	GND-J2	BP	BP return	Backplane-only position
P2.W11.h	GND	GND	Return	Module signal return
P2.W11.i	SPI0_CS2*	RES	SPI reserved	Reserved; no command service
P2.W12.a	GND	GND	Return	Module signal return
P2.W12.b	GND-J2	BP	BP return	Backplane-only position
P2.W12.c	RESERVED	RES	Reserved	No data service allocated
P2.W12.d	RESERVED	RES	Reserved	No data service allocated
P2.W12.e	GND	GND	Return	Module signal return
P2.W12.f	GND-J2	BP	BP return	Backplane-only position
P2.W12.g	RESERVED	RES	Reserved	No data service allocated
P2.W12.h	RESERVED	RES	Reserved	No data service allocated
P2.W12.i	GND	GND	Return	Module signal return

A.12 P2 | Wafers 13-16

Connector reference | Directions relative to storage card

Position	Signal	Dir	Function	Connection note
P2.W13.a	AUX_CLK_A_P	IN	Clock	Source/receiver: electrical interface
P2.W13.b	AUX_CLK_A_N	IN	Clock	Source/receiver: electrical interface
P2.W13.c	GND-J2	BP	BP return	Backplane-only position
P2.W13.d	GND	GND	Return	Module signal return
P2.W13.e	REF_CLK_A_P	IN	Clock	Source/receiver: electrical interface
P2.W13.f	REF_CLK_A_N	IN	Clock	Source/receiver: electrical interface
P2.W13.g	GND-J2	BP	BP return	Backplane-only position
P2.W13.h	GND	GND	Return	Module signal return
P2.W13.i	SYSRESET_A*	IN	Control	Behaviour: electrical interface
P2.W14.a	GND	GND	Return	Module signal return
P2.W14.b	GND-J2	BP	BP return	Backplane-only position
P2.W14.c	AUX_CLK_B_P	IN	Clock	Source/receiver: electrical interface
P2.W14.d	AUX_CLK_B_N	IN	Clock	Source/receiver: electrical interface
P2.W14.e	GND	GND	Return	Module signal return
P2.W14.f	GND-J2	BP	BP return	Backplane-only position
P2.W14.g	REF_CLK_B_P	IN	Clock	Source/receiver: electrical interface
P2.W14.h	REF_CLK_B_N	IN	Clock	Source/receiver: electrical interface
P2.W14.i	GND	GND	Return	Module signal return
P2.W15.a	SM1_B	I/O	Mgmt	Bus pairing: interface schedule
P2.W15.b	SM0_B	I/O	Mgmt	Bus pairing: interface schedule
P2.W15.c	GND-J2	BP	BP return	Backplane-only position
P2.W15.d	GND	GND	Return	Module signal return
P2.W15.e	SM3_B	I/O	Mgmt	Bus pairing: interface schedule
P2.W15.f	SM2_B	I/O	Mgmt	Bus pairing: interface schedule
P2.W15.g	GND-J2	BP	BP return	Backplane-only position
P2.W15.h	GND	GND	Return	Module signal return
P2.W15.i	SYSRESET_B*	IN	Control	Behaviour: electrical interface
P2.W16.a	GND	GND	Return	Module signal return
P2.W16.b	GND-J2	BP	BP return	Backplane-only position
P2.W16.c	SM1_A	I/O	Mgmt	Bus pairing: interface schedule
P2.W16.d	SM0_A	I/O	Mgmt	Bus pairing: interface schedule
P2.W16.e	GND	GND	Return	Module signal return
P2.W16.f	GND-J2	BP	BP return	Backplane-only position
P2.W16.g	SM3_A	I/O	Mgmt	Bus pairing: interface schedule
P2.W16.h	SM2_A	I/O	Mgmt	Bus pairing: interface schedule
P2.W16.i	GND	GND	Return	Module signal return