PSU-Polar-3U User Guide

SOSA-aligned 3U VPX 600 W-class Power Supply Module

Electrical, Mechanical, Management & Environmental Interfaces

Document Specification

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Version	Date	Author	Description
1.0	Feb. 2025	A.A	Initial release interface definition for the PSU-Polar-3U 600 W-class 3U VPX power supply module.
1.1	Aug. 2025	A.A	Updated to the dual-branch internal power architecture. Documents two filtered input branches feeding two +12 V conversion sections and two +3.3 V_AUX conversion sections. Adds branch and converter-section telemetry, six temperature sensors, expanded FDIR fault set, authoritative connector pin map, and released-product specifications.
1.2	Jan. 2026	A.A	Minor customer-facing clarity update. Adds a management controller and software overview, an expanded power-state model, clarified input protection and dual-branch architecture, a customer-safe input-current telemetry and isolation explanation, an improved output-filtering description, and a six-line VPX P0 visual pin map with a P0 functional allocation table. Product baseline, ratings, and pin map are unchanged.
1.3	June 2026	A.A	Updates the released output allocation to 550 W on +12 V_MAIN and 50 W on +3.3 V_AUX, preserving the 600 W-class product rating while aligning the auxiliary rail with the LP2 connector current capability. Updates current-carrying ratings, diagrams, pin-map ratings, verification limits, and customer-facing power-allocation language.

Abbreviations

AUX	Auxiliary output rail (+3.3 V_AUX)
ESD	Electrostatic discharge
EMI	Electromagnetic interference
FDIR	Fault detection, isolation, and recovery
FRU	Field-replaceable unit
GA	Geographic address
ICD	Interface control document
IPMB	Intelligent platform management bus
MAIN	Main output rail (+12 V_MAIN)
ORing	Output redundancy combining with reverse-current blocking
OVP	Overvoltage protection
RH	Relative humidity
SOSA	Sensor Open Systems Architecture
UART	Universal asynchronous receiver/transmitter (service serial interface)
VDC	Volts, direct current
VITA	VMEbus International Trade Association
VPX	OpenVPX backplane and module ecosystem

1. Introduction

1.1 Purpose and Scope

This user guide defines the electrical, mechanical, control, management, redundancy, operating, and environmental interfaces of the PSU-Polar-3U power supply module. It is the released interface reference for chassis designers, backplane designers, system integrators, firmware engineers, verification engineers, and end users who integrate the module into a VPX/SOSA-aligned system.

PSU-Polar-3U is a released aerospace and space VPX power product. The values in this guide are product specifications. The module is rated and qualified to the limits stated in this document.

1.2 How to Use This Guide

Sections 2 through 4 define the product architecture, electrical interface, and connector pin map. Sections 5 through 7 define operating behaviour, management, monitoring, and fault handling. Sections 8 through 12 define grounding, mechanical and thermal integration, environmental specifications, handling, and verification. Sections 13 through 16 provide installation guidance, troubleshooting, support information, and related documents.

1.3 Product Overview

PSU-Polar-3U is a conduction-cooled, SOSA-aligned 3U VPX 600 W-class power supply module for nominal 28 VDC systems. The module accepts a 16–36 VDC input and provides two isolated output rails for a SOSA-aligned VPX payload backplane. It implements input protection, controlled inrush, dual filtered input branches, isolated conversion, active MOSFET output ORing, comprehensive telemetry, local FDIR, and a CAVU on-board management controller with dual IPMB-style management buses.

The module provides only the SOSA-aligned two-rail output set: +12 V_MAIN and +3.3 V_AUX. Legacy VITA 62 rails are not implemented: there is no +5 V rail, no +3.3 V main payload rail, no +12 V_AUX rail, and no -12 V_AUX rail.

Output rail	Nominal voltage	Rated current	Rated power	Function
+12 V_MAIN	+12.0 VDC	46 A	550 W	Main payload power rail
+3.3 V_AUX	+3.3 VDC	15 A	50 W	Auxiliary, management, and standby rail
Total	—	—	600 W class	Released product power class

Table 1 — PSU-Polar-3U output rail summary.

2. System Architecture

2.1 Top-Level System Block Diagram

The module accepts protected input power, measures total input current, and distributes power through a protected split node to two filtered input branches. Each branch supplies isolated conversion sections that generate the +12 V_MAIN and +3.3 V_AUX rails. The rails are combined through active MOSFET ORing and presented to the VPX backplane. Solid paths represent the power flow; dashed paths represent status and control exchanged with the on-board management controller

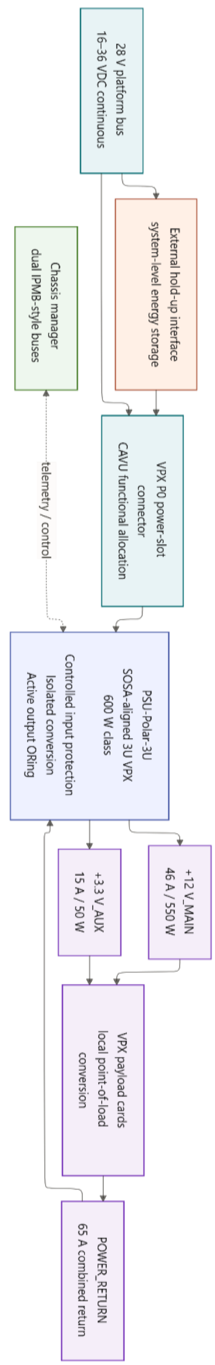

Figure 1 — PSU-Polar-3U top-level system block diagram

2.2 Dual-Branch Internal Power Architecture

The 600 W-class rating is delivered by a balanced dual-branch architecture. The protected input path feeds a split node that supplies two filtered input branches, Branch A and Branch B. Each branch is rated for 22 A continuous and supplies one +12 V conversion section and one +3.3 V_AUX conversion section.

The +12 V_MAIN rail is generated by two 23 A-class conversion sections. The +3.3 V_AUX rail is generated by balanced auxiliary conversion sections that support the 15 A combined auxiliary-rail rating. The conversion-section outputs are combined through controlled balancing and active MOSFET ORing to form the +12 V_MAIN and +3.3 V_AUX output rails. The management controller monitors branch-current balance, converter-section status, ORing status, and thermal status across both branches.

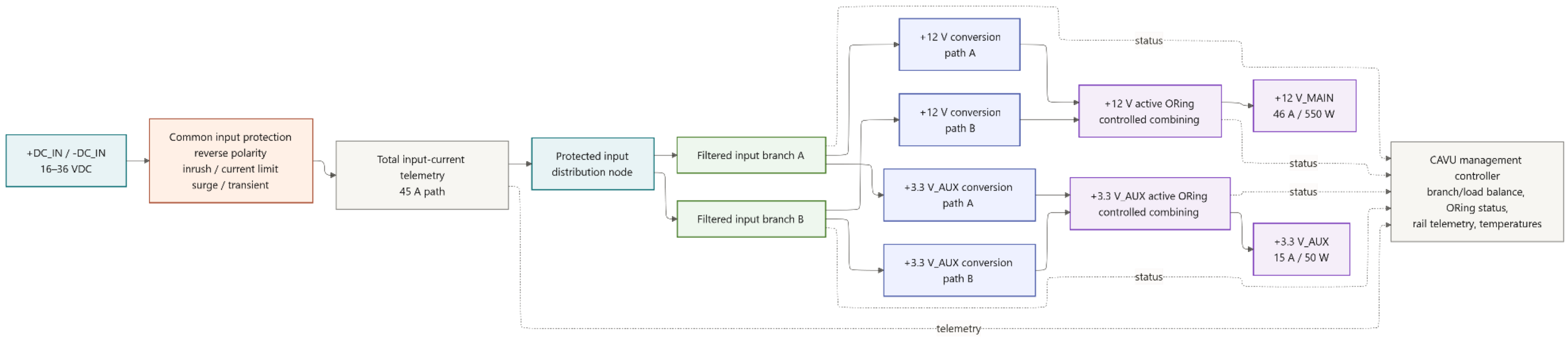

Figure 2 — Dual-branch internal power architecture.

Branch	Conversion section	Section rating	Combined rail contribution
Branch A	+12 V conversion section A	12 V / 23 A	One half of +12 V_MAIN (46 A)
Branch A	+3.3 V_AUX conversion section A	Balanced AUX share	Supports the 15 A combined AUX rail
Branch B	+12 V conversion section B	12 V / 23 A	One half of +12 V_MAIN (46 A)
Branch B	+3.3 V_AUX conversion section B	Balanced AUX share	Supports the 15 A combined AUX rail

Table 2 — Branch-to-section allocation.

2.3 Applicable Interface Standards

Area	Interface
Mechanical ecosystem	3U VPX conduction-cooled power module
Power interface	VITA 62 VPX power supply module interface
Management interface	VITA 46.11 platform management
Architecture framework	VITA 65 / OpenVPX and the SOSA Technical Standard
Rail philosophy	SOSA-aligned two-rail output structure (+12 V_MAIN, +3.3 V_AUX)
System management bus	Dual redundant IPMB-style management buses (IPMB-A, IPMB-B)

3. Electrical Interface

3.1 Electrical Interface Summary

Input voltage range	**16–36 VDC continuous**
Nominal input voltage	28 VDC
Input path rating	45 A continuous
Main output	+12 V_MAIN at 46 A (550 W)
Auxiliary output	+3.3 V_AUX at 15 A (50 W)
Total output	600 W class
Product class	600 W class
Output isolation	500 VDC minimum input-to-output, input-to-case, and output-to-case
Interface ESD	±8 kV contact and ±15 kV air
Inrush control	Integrated controlled-start input stage
Reverse-polarity protection	Integrated low-loss reverse-input protection
Output redundancy	Active MOSFET ORing on both output rails
Hold-up	External hold-up interface supported; no internal long-duration hold-up shall be assumed

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3.2 Input Power

Minimum continuous input	16 VDC
Nominal input	28 VDC
Maximum continuous input	36 VDC
Input path rating	45 A continuous
Inrush	Controlled-start input stage limits inrush into the filter and conversion stages
Input current measurement	Total input-current measurement path rated 45 A continuous, located before the branch split
Input undervoltage	Module reports the event and inhibits or shuts down outputs in a controlled manner when the operating limit is exceeded
Input overvoltage	Module protects itself and reports the event

The total input-current measurement path is located after the input protection stage and before the branch split, so it reports true module input current independent of branch balance.

3.3 Output Power

3.3.1 +12 V_MAIN Output

Nominal voltage	+12.0 VDC
Rated current	46 A
Rated power	550 W
Generation	Two 23 A-class conversion sections, one per filtered input branch
Remote sense	Supported (A8 / D8)
Output ORing	Active MOSFET ORing, 46 A continuous path
Protection	Overcurrent, overvoltage, undervoltage, and overtemperature protection with management reporting

3.3.2 +3.3 V_AUX Output

Nominal voltage	+3.3 VDC
Rated current	15 A
Rated power	50 W
Generation	Balanced auxiliary conversion sections across the two filtered input branches
Remote sense	Supported (B8 / D8)
Output ORing	Active MOSFET ORing, 15 A continuous path
Function	Auxiliary, management, and standby power rail
Protection	Overcurrent, overvoltage, undervoltage, and overtemperature protection with management reporting

The module provides a released 600 W-class output allocation consisting of 550 W on +12 V_MAIN and 50 W on +3.3 V_AUX. Loads shall not exceed either rail current rating or the total module thermal rating.

3.4 Current-Carrying Ratings

Current path	Continuous rating	Note
VPX input path	45 A	Covers 600 W output at 16 V low line with conversion-loss margin
Filtered input branch A	22 A	Carries one balanced share of total input power
Filtered input branch B	22 A	Carries one balanced share of total input power
+12 V converter section A	12 V / 23 A	One half of the +12 V_MAIN rail
+12 V converter section B	12 V / 23 A	One half of the +12 V_MAIN rail
+3.3 V_AUX converter section A	Balanced AUX share	Supports the 15 A combined AUX rail
+3.3 V_AUX converter section B	Balanced AUX share	Supports the 15 A combined AUX rail
+12 V_MAIN ORing path	46 A	Supports full main rail current
+3.3 V_AUX ORing path	15 A	Supports full AUX rail current
POWER_RETURN combined path	65 A	Supports simultaneous 46 A main and 15 A AUX return current
Total input-current measurement path	45 A	Measurement element and copper support full low-line input current

Table 3 — Current-carrying ratings.

3.5 Input Protection and Dual-Branch Architecture

The module implements a protected input path that feeds a single split node. The protected input path provides service fusing, transient and surge suppression, reverse-polarity protection, controlled inrush, and input current limiting before the split node. After the split node, the module provides two filtered input branches, Branch A and Branch B.

Each filtered input branch is rated for 22 A continuous. Branch A supplies one +12 V conversion section and one +3.3 V_AUX conversion section; Branch B supplies one +12 V conversion section and one +3.3 V_AUX conversion section. This balanced arrangement keeps low-line input current distributed across both branches so that neither branch exceeds its 22 A continuous rating at full load.

Stage	Function
Protected input path	Service fusing, surge/transient suppression, reverse-polarity protection, controlled inrush, and input current limiting ahead of the split node
Split node	Single protected distribution point that feeds Branch A and Branch B
Filtered input branch A	22 A continuous filtered branch feeding +12 V conversion section A and +3.3 V_AUX conversion section A
Filtered input branch B	22 A continuous filtered branch feeding +12 V conversion section B and +3.3 V_AUX conversion section B
Branch-balance monitoring	The management controller reports branch load and branch-balance status

3.6 Input-Current Telemetry and Isolation

The module measures total input current before the branch split, so reported input current reflects true module input current independently of branch balance. The input measurement is on the primary input side of the isolation boundary, and the management controller is on the logic side. Primary-side telemetry therefore crosses the isolation boundary through isolated telemetry circuitry, and the primary-side measurement is supported by an isolated low-power housekeeping supply.

The management interface reports input voltage, input current, input power, and branch load and branch-balance status. The module maintains at least 500 VDC isolation between the input return and the output and signal domains.

Telemetry / domain	Behaviour
Input current	Measured before the Branch A / Branch B split to report true module input current
Primary-side telemetry	Crosses the isolation boundary through isolated telemetry circuitry
Reported input quantities	Input voltage, input current, input power, and branch load / balance status
Isolation	500 VDC minimum between input return and the output and signal domains

3.7 Output Filtering and ORing

Each conversion section provides local damped output filtering. The two +12 V conversion sections and the two +3.3 V_AUX conversion sections are combined through controlled balancing and active MOSFET ORing. A final output filter and the remote-sense point are provided at the VPX output interface. The ORing stage provides reverse-current blocking, which supports dual-module redundant operation.

Rail	Local filter	Combining	Final filter and sense
+12 V_MAIN	Damped local output filtering per conversion section	Two +12 V sections combined through controlled balancing and active MOSFET ORing	Final filtering and remote sense at the VPX output interface
+3.3 V_AUX	Damped local output filtering per conversion section	Two +3.3 V_AUX sections combined through controlled balancing and active MOSFET ORing	Final filtering and remote sense at the VPX output interface

System-level item	Guidance
Backplane decoupling	Use local decoupling near load cards according to the load-card requirements
External bulk capacitance	Up to 5 mF on +12 V_MAIN and up to 10 mF on +3.3 V_AUX may be added at system level
External LC filters	External filters shall be damped to avoid resonance with the module output stage
Remote sense	Sense is taken after ORing and final filtering at the VPX output interface

4. VPX Connector Interface and Pin Map

4.1 Connector Authority Statement

This section defines the CAVU PSU-Polar-3U SOSA-aligned VPX power-slot allocation. Backplanes using PSU-Polar-3U shall route contacts according to this guide and the CAVU connector interface drawing. This allocation is the authoritative pin map for the product.

4.2 Power Contacts

Contact	Signal	Direction	Description
P1	-DC_IN	Input	Input power return
P2	+DC_IN	Input	16–36 VDC input power
LP1	CHASSIS	Chassis	Chassis and frame reference
P3	+12 V_MAIN	Output	Main +12 V output, paralleled with P6
P6	+12 V_MAIN	Output	Main +12 V output, paralleled with P3
P4	POWER_RETURN	Return	Output power return
P5	POWER_RETURN	Return	Output power return
LP2	+3.3 V_AUX	Output	Auxiliary +3.3 V output

4.3 Sense Contacts

Contact	Signal	Direction	Description
A8	+12 V_SENSE	Input to module	Remote sense for +12 V_MAIN
B8	+3.3 V_AUX_SENSE	Input to module	Remote sense for +3.3 V_AUX
D8	SENSE_RETURN	Input to module	Remote sense return

Remote sense shall be routed from the regulated load point or designated backplane sense point as a Kelvin pair with SENSE_RETURN. Sense lines shall not be used as load-current conductors.

4.4 Control and Status Contacts

Contact	Signal	Direction	Active	Description
D2	ENABLE*	Input to module	Low	Enables module input and management-controlled power sequence
C2	INHIBIT*	Input to module	Low	Inhibits +12 V_MAIN while allowing AUX behaviour per state definition
B2	FAIL*	Output from module	Low	Module fault indication
D6	SYSRESET*	Profile-defined	Low	System reset / reset-status interface
D7	SIGNAL_RETURN	Reference	—	Signal reference for management/control pins
A5	GA0*	Input to module	Low	Geographic address bit 0
B5	GA1*	Input to module	Low	Geographic address bit 1
C3	NED	Input to module	Profile	Emergency shutdown input
D3	NED_RETURN	Reference	—	Emergency shutdown input reference

4.5 Management-Bus Contacts

Contact	Signal	Direction	Description
C5	IPMB-A_SCL	Bidirectional	Primary management clock
D5	IPMB-A_SDA	Bidirectional	Primary management data
A6	IPMB-B_SCL	Bidirectional	Redundant management clock
B6	IPMB-B_SDA	Bidirectional	Redundant management data

The module operates with either management bus available. Loss of one management bus does not, by itself, disable power output.

4.6 No-Connect Contacts

Contacts	Treatment
A4, B4, C4, D4	No electrical connection. Leave unconnected; do not repurpose for private or proprietary signals.

4.7 Six-Line Visual Pin Map

The visual pin map presents the CAVU PSU-Polar-3U SOSA-aligned VPX power-slot allocation in six short lines so it can be reproduced cleanly on A4 reports and schematic notes without wrapping.

Line	VPX P0 allocation
1	Power input: P1 = -DC_IN, P2 = +DC_IN, LP1 = CHASSIS
2	Main output: P3 = +12 V_MAIN, P6 = +12 V_MAIN, P4/P5 = POWER_RETURN
3	AUX and sense: LP2 = +3.3 V_AUX, A8 = +12 V_SENSE, B8 = +3.3 V_AUX_SENSE, D8 = SENSE_RETURN
4	Control/status: D2 = ENABLE*, C2 = INHIBIT*, B2 = FAIL*, D6 = SYSRESET*
5	Management/GA: A5 = GA0*, B5 = GA1*, C5/D5 = IPMB-A, A6/B6 = IPMB-B
6	Emergency/NC: C3 = NED, D3 = NED_RETURN, D7 = SIGNAL_RETURN, A4/B4/C4/D4 = NC

Six-line visual pin map (CAVU PSU-Polar-3U SOSA-aligned power-slot allocation).

4.8 Functional Pin Map

The functional pin map below presents the connector allocation as grouped interface domains. It complements the VPX P0 connector functional allocation in Section 4.9 and the full pin map table in Section 4.10, together with the CAVU connector interface drawing.

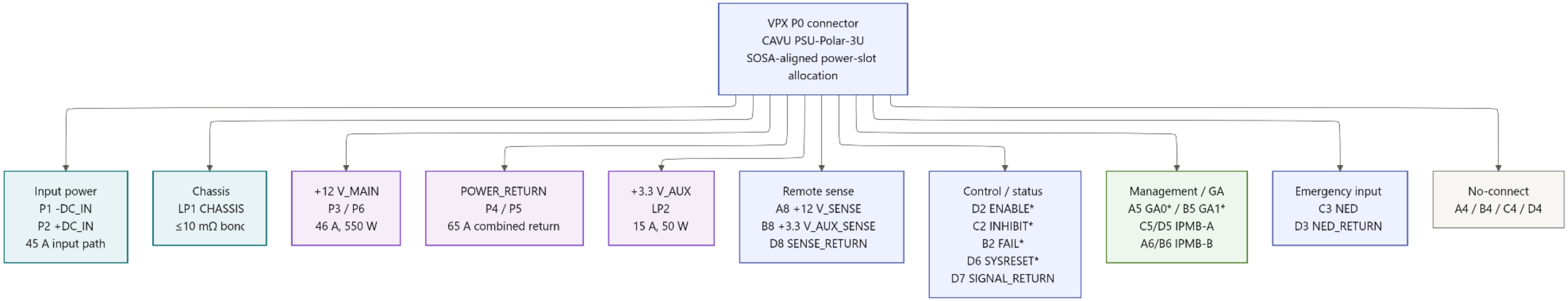

Figure 3 — VPX connector functional pin map (CAVU PSU-Polar-3U SOSA-aligned power-slot allocation).

4.9 VPX P0 Connector Functional Allocation

The VPX P0 connector functional allocation groups the power-slot contacts by function and states the design rating or rule for each group. This is the CAVU PSU-Polar-3U SOSA-aligned VPX power-slot allocation; backplanes shall route contacts according to this guide and the CAVU connector interface drawing.

Functional group	Contacts	Signals	Rating / rule
Input power	P1, P2	-DC_IN, +DC_IN	16–36 VDC, 45 A continuous input path
Chassis / frame	LP1	CHASSIS	Chassis bond ≤10 mΩ to module frame / conduction edge
Main output rail	P3, P6	+12 V_MAIN	+12.0 VDC, 46 A combined, 550 W
Output power return	P4, P5	POWER_RETURN	65 A combined return path
Auxiliary rail	LP2	+3.3 V_AUX	+3.3 VDC, 15 A, 50 W
Remote sense	A8, B8, D8	+12 V_SENSE, +3.3 V_AUX_SENSE, SENSE_RETURN	High-impedance sense lines; not load-current paths
Control and status	D2, C2, B2, D6	ENABLE*, INHIBIT*, FAIL*, SYSRESET*	3.3 V logic / signalling, ESD-protected
Geographic address	A5, B5	GA0*, GA1*	Sampled by the management controller at startup
Management buses	C5, D5, A6, B6	IPMB-A_SCL/SDA, IPMB-B_SCL/SDA	Open-drain 3.3 V management buses
Emergency input	C3, D3	NED, NED_RETURN	Emergency shutdown input and return
Signal reference	D7	SIGNAL_RETURN	Signal reference only; not a load-current return
Reserved contacts	A4, B4, C4, D4	NC	No electrical connection

Table 4 — VPX P0 connector functional allocation.

4.10 Full Pin Map Table

Contact	Signal	Group	Direction	Active	Rating / limit	Use
P1	-DC_IN	Input power	Input	—	45 A module input path with P2	Input return
P2	+DC_IN	Input power	Input	—	16–36 VDC continuous, 45 A maximum input current	Input power
LP1	CHASSIS	Chassis	Chassis	—	Chassis bond ≤10 mΩ to module frame	Frame, shield, chassis reference
P3	+12 V_MAIN	Output power	Output	—	+12 V, 46 A combined with P6	Main +12 V rail
P6	+12 V_MAIN	Output power	Output	—	+12 V, 46 A combined with P3	Main +12 V rail
P4	POWER_RETURN	Output return	Return	—	65 A combined output-return path with P5	Output power return
P5	POWER_RETURN	Output return	Return	—	65 A combined output-return path with P4	Output power return
LP2	+3.3 V_AUX	Output power	Output	—	+3.3 V, 15 A	Auxiliary +3.3 V rail
A8	+12 V_SENSE	Remote sense	Input to module	—	High-impedance sense, <10 mA, ESD-protected	+12 V remote sense
B8	+3.3 V_AUX_SENSE	Remote sense	Input to module	—	High-impedance sense, <10 mA, ESD-protected	+3.3 V_AUX remote sense
D8	SENSE_RETURN	Remote sense	Input to module	—	High-impedance sense return, <10 mA, ESD-protected	Sense return
D2	ENABLE*	Control	Input to module	Low	3.3 V logic, ESD ±8 kV contact / ±15 kV air	Module enable
C2	INHIBIT*	Control	Input to module	Low	3.3 V logic, ESD ±8 kV contact / ±15 kV air	Main rail inhibit
B2	FAIL*	Status	Output from module	Low	Open-drain, 3.3 V logic, sink ≤8 mA	Module fault indication
D6	SYSRESET*	Control/status	Profile-defined	Low	3.3 V logic, ESD ±8 kV contact / ±15 kV air	System reset / reset status
D7	SIGNAL_RETURN	Signal reference	Reference	—	Signal return; not a power return	Control/management signal reference
A5	GA0*	Address	Input to module	Low	3.3 V logic, sampled at startup	Geographic address bit 0
B5	GA1*	Address	Input to module	Low	3.3 V logic, sampled at startup	Geographic address bit 1

C5	IPMB-A_SCL	Management	Bidirectional	—	Open-drain 3.3 V, 100 kHz default / 400 kHz maximum	Primary management clock
D5	IPMB-A_SDA	Management	Bidirectional	—	Open-drain 3.3 V, 100 kHz default / 400 kHz maximum	Primary management data
A6	IPMB-B_SCL	Management	Bidirectional	—	Open-drain 3.3 V, 100 kHz default / 400 kHz maximum	Redundant management clock
B6	IPMB-B_SDA	Management	Bidirectional	—	Open-drain 3.3 V, 100 kHz default / 400 kHz maximum	Redundant management data
C3	NED	Emergency input	Input to module	Profile	3.3 V logic, ≤10 µs response after qualified assertion	Emergency shutdown input
D3	NED_RETURN	Emergency ref.	Reference	—	Emergency-input return; not a power return	Emergency input return
A4	NC	No-connect	—	—	No electrical connection	Leave unconnected
B4	NC	No-connect	—	—	No electrical connection	Leave unconnected
C4	NC	No-connect	—	—	No electrical connection	Leave unconnected
D4	NC	No-connect	—	—	No electrical connection	Leave unconnected

Table 5 — Full pin map with per-contact ratings and limits.

5. Operating Behaviour

5.1 Power-State Model

The module implements a managed power-state model. The power-state manager in the on-board management controller selects the active state from input validity, the ENABLE* and INHIBIT* control pins, detected faults, and recovery policy, and records every state transition in the nonvolatile event log. The customer-facing states are summarised below.

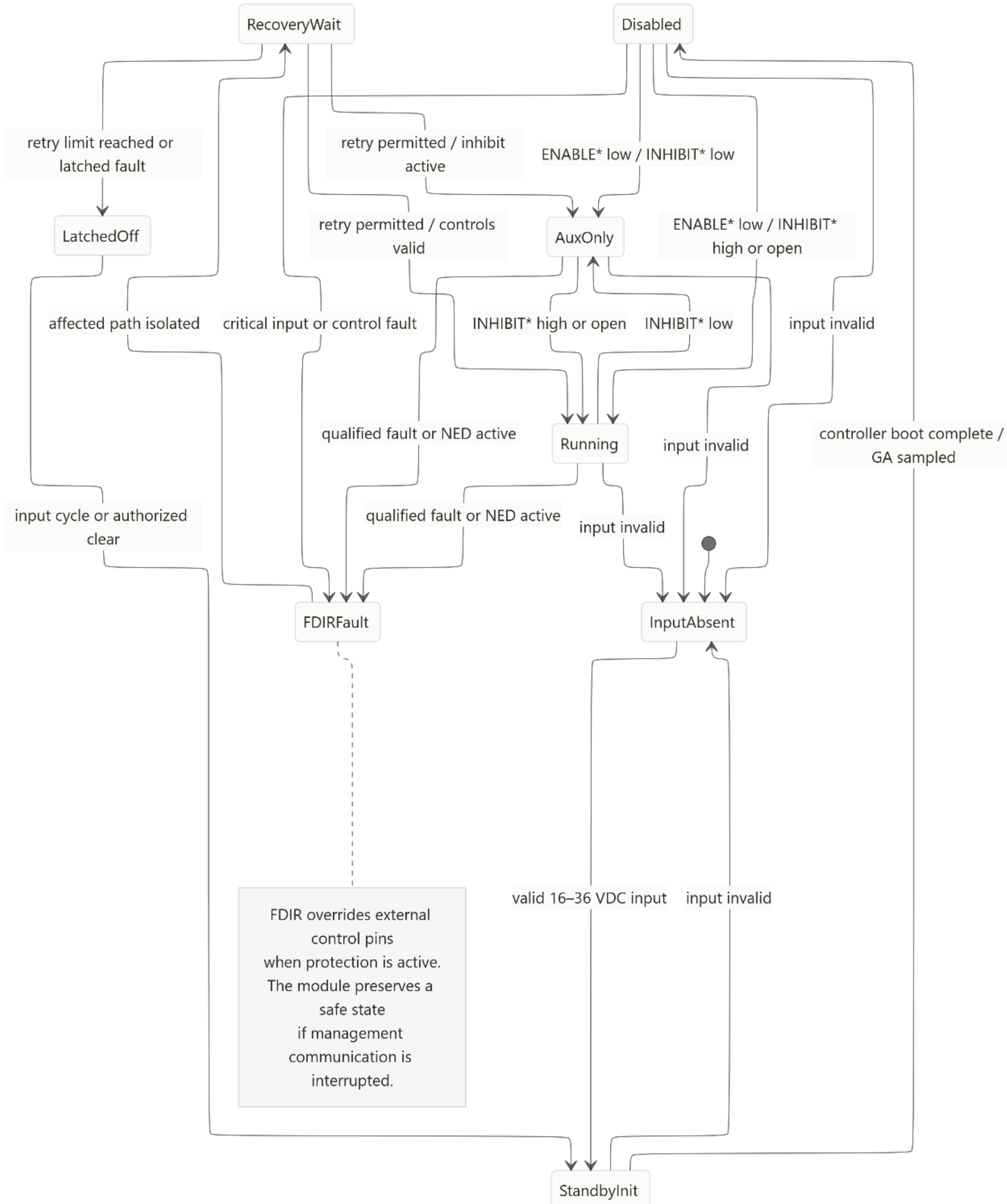

Figure 8 — PSU-Polar-3U power-state model.

State	Description
InputAbsent	No valid input is present at +DC_IN / -DC_IN; the module is unpowered and both rails are off.
StandbyInit	Input is valid and within 16–36 VDC; the management controller initialises, samples the geographic address pins, and brings up the management buses before any main rail is enabled.
Disabled	Input is valid but ENABLE* is de-asserted; both +12 V_MAIN and +3.3 V_AUX outputs are held off under management control.
AuxOnly	ENABLE* is asserted with INHIBIT* asserted; +3.3 V_AUX is supplied for auxiliary, management, and standby loads while +12 V_MAIN remains off.
Running	ENABLE* asserted and INHIBIT* released; both +12 V_MAIN and +3.3 V_AUX are supplied within rating and full telemetry is reported.
FDIRFault	A fault has been detected and classified; the module applies the configured FDIR response, asserts FAIL*, and logs the event.
RecoveryWait	The module is holding after a recoverable fault, waiting for the recovery policy timer or an external clear before attempting a controlled restart.
LatchedOff	A non-recoverable or repeated fault has latched the affected output off; the module remains off until input is removed and reapplied or an authorised reset is received.

Hardware fast protection acts independently of the power-state manager. Local protection latches an output off on a hardware-speed event regardless of management-bus state, and the power-state manager reflects the resulting condition in the reported state and event log.

5.2 Control-State Behaviour

Control-state behaviour is driven by input validity, the ENABLE* and INHIBIT* control pins, detected faults, and recovery policy.

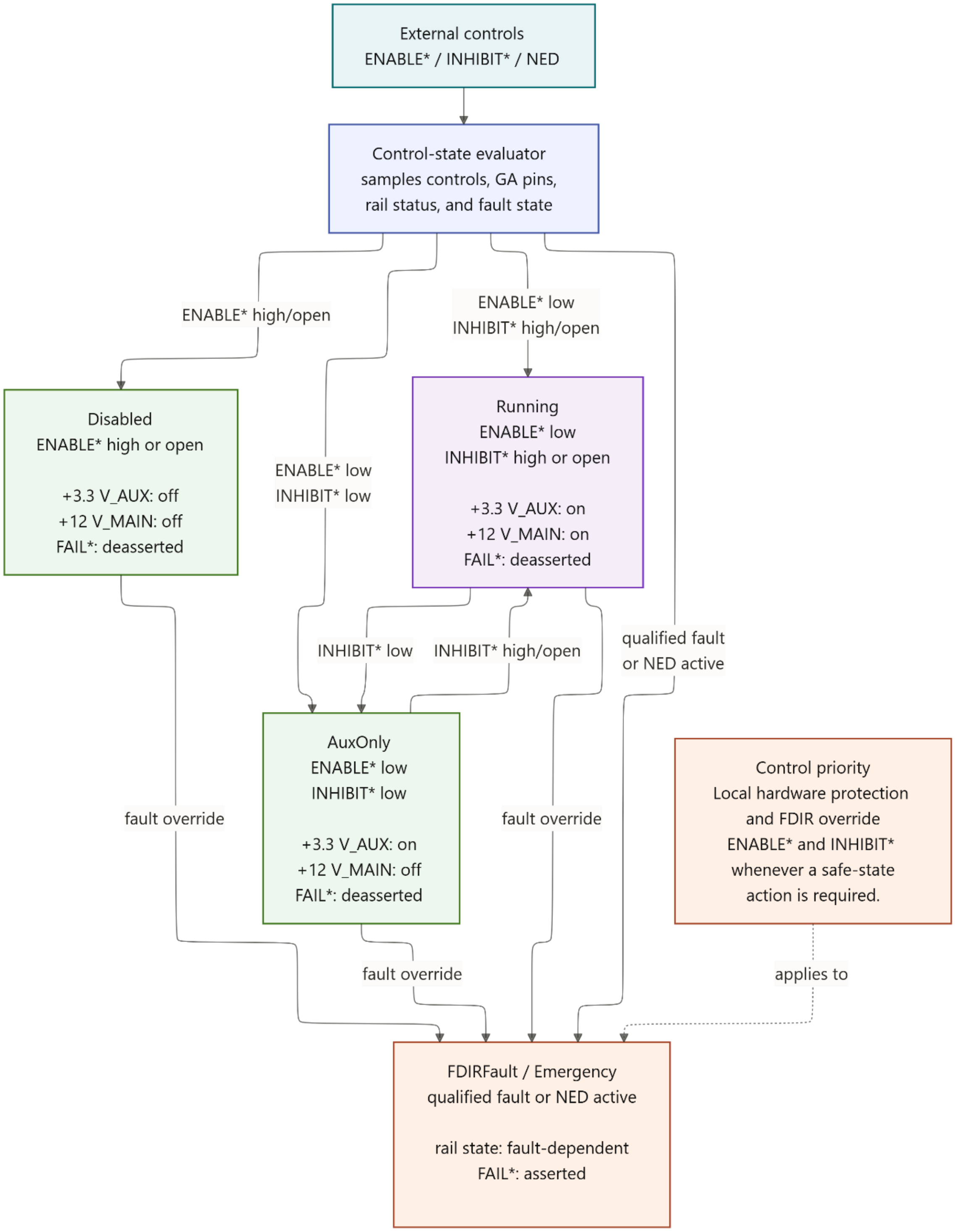

Figure 4 — Control-state behaviour.

ENABLE*	INHIBIT*	+3.3 V_AUX	+12 V_MAIN	State
High/open	Any	Off	Off	Disabled
Low	Low	On	Off	AUX only
Low	High/open	On	On	Running
Any	Any	Fault-dependent	Fault-dependent	FDIR-managed fault

The management controller samples the geographic address pins at startup, publishes module identity over both management buses, and records all control-state transitions in the event log.

5.3 Power-Up Sequence

1. Input power is applied to +DC_IN / -DC_IN.
2. The input protection and controlled-inrush stage activate.
3. The on-board management controller initialises and samples the geographic address pins.
4. The management buses become active and the module publishes its identity.
5. +3.3 V_AUX is enabled when permitted by the ENABLE* and INHIBIT* state.
6. +12 V_MAIN is enabled when ENABLE* is asserted and INHIBIT* is released.
7. The module reports rail-good status and normal telemetry.

5.4 Redundant Operation

The module supports dual-module redundant operation when two identical PSU-Polar-3U modules feed the same VPX backplane power rails. Each module provides active MOSFET output ORing, independent FDIR, a unique geographic address, and independent IPMB presence.

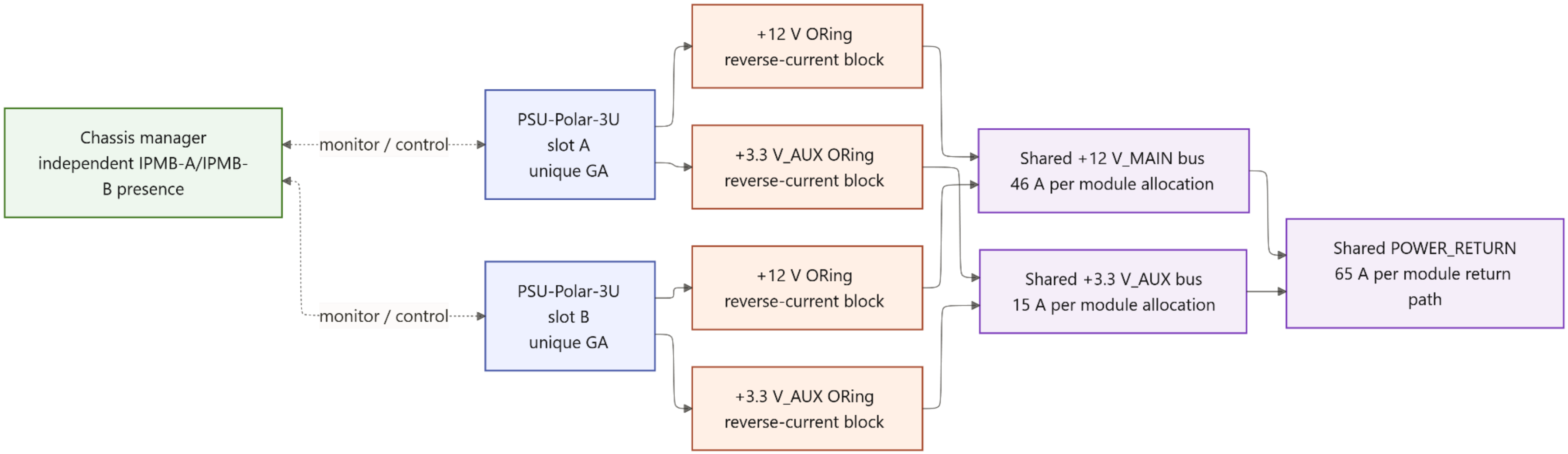

Figure 6 — Dual-module redundant operation.

Requirement	Description
Backplane support	Connect the corresponding output rails from both power slots to common power buses
ORing	Each module blocks reverse current from the shared backplane rails
Addressing	Each module has a unique geographic address
Management	The chassis manager monitors both modules independently over IPMB-A and IPMB-B
Fault isolation	A failed module is isolated from the shared rails by its ORing stage

6. Management and Monitoring Interface

The CAVU on-board management controller supervises input power, output rails, branch balance, converter-section status, temperatures, protection status, fault handling, event logs, and management-bus communication.

6.1 CAVU Management Controller and Software Overview

The PSU-Polar-3U integrates an on-board CAVU management controller that supervises the module at the interface level. The controller presents a managed power-supply endpoint to the chassis manager and coordinates monitoring, protection reporting, power-state management, and controlled firmware maintenance. The overview below is interface-level; it describes the functions the customer interacts with, not internal implementation.

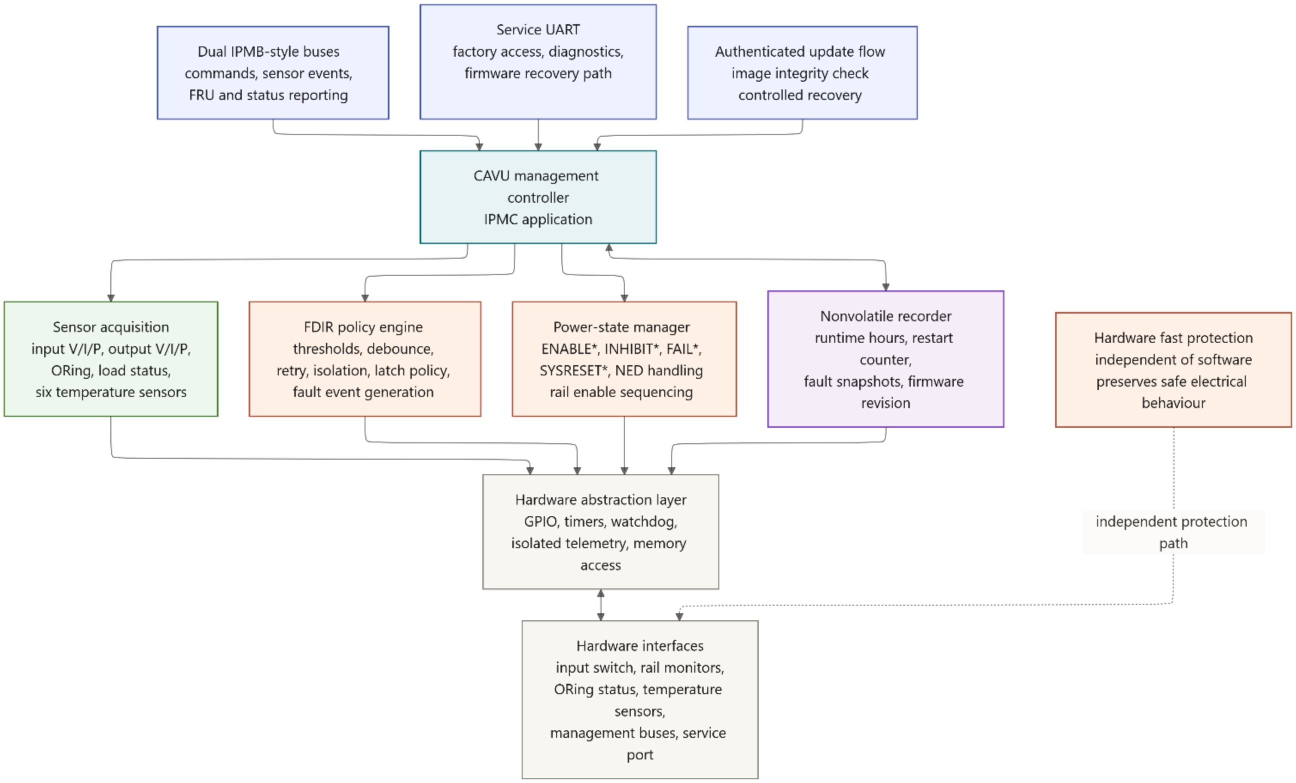

Figure 7 — CAVU management controller and software overview.

Function	Description
On-board management controller	A dedicated CAVU management controller supervises the module and presents a managed power-supply endpoint to the chassis manager.
Dual IPMB-style management buses	The controller communicates over two redundant IPMB-style management buses (IPMB-A and IPMB-B); loss of one bus does not interrupt module operation.
Sensor acquisition	The controller acquires input, rail, branch, converter-section, and temperature measurements and makes them available as telemetry.
FDIR policy engine	A fault-detection, isolation, and recovery policy engine classifies detected faults and applies the configured recovery policy.
Power-state manager	A power-state manager selects the active power state from input validity, the ENABLE* and INHIBIT* pins, faults, and recovery policy, and sequences the rails accordingly.
Nonvolatile fault/event recorder	A nonvolatile recorder stores fault and event records, runtime hours, and restart counters so that history is retained across power cycles.
Authenticated firmware update and recovery	Firmware update and recovery use an authenticated image and a controlled maintenance state; the management bus is the preferred update path and a service serial bootloader provides the recovery path.
Hardware fast protection (independent)	Hardware fast protection operates independently of the controller and software; local protection latches an affected output off at hardware speed regardless of management-bus state.

Local protection and FDIR do not depend on continuous management-bus communication. The module protects itself and applies its recovery policy autonomously, and the management interface reports the resulting status.

6.2 Management-Bus Behaviour

Feature	Specification
Bus topology	Dual redundant IPMB-style buses (IPMB-A, IPMB-B)
Address source	Geographic address pins GA0*, GA1*
Bus fault behaviour	Loss of one bus does not shut down the module
Default bus speed	100 kHz
Maximum bus speed	400 kHz
Electrical style	3.3 V open-drain clock and data
Pull-ups	Provided by the backplane or chassis manager

6.3 Monitoring Communication Interface

The management interface uses an IPMB-style request/response transaction model over the redundant I2C-compatible buses. The module acts as a managed power-supply endpoint and the chassis manager acts as the bus master for monitoring and control.

6.3.1 Request Frame Format

Byte field	Description
Responder address	Module management address derived from geographic address pins
NetFn / LUN	Network function and logical unit number
Header checksum	Two's-complement checksum over responder address and NetFn/LUN
Requester address	Chassis manager address
Request sequence / LUN	Request sequence number and requester logical unit number
Command	Command code
Data bytes	Optional command payload
Data checksum	Two's-complement checksum over requester address through final data byte

6.3.2 Response Frame Format

Byte field	Description
Requester address	Chassis manager address
NetFn response / LUN	Response network function and logical unit number
Header checksum	Two’s-complement checksum over requester address and response NetFn/LUN
Responder address	Module management address
Request sequence / LUN	Echoed request sequence number and logical unit number
Command	Echoed command code
Completion code	Command completion result
Data bytes	Optional response payload
Data checksum	Two’s-complement checksum over responder address through final response data byte

6.3.3 Example Management Frame

The following illustrative Get Device ID transaction uses example addresses assigned by the system profile.

Transaction	Example bytes	Meaning
Request	42 18 A6 20 00 01 DF	Request from chassis manager address 20 to module address 42, application NetFn, command 01
Response	20 1C C4 42 00 01 00 01 00 BC	Response with completion code 00 and two example data bytes

6.4 Service Serial Debug and Firmware Update Interface

The module provides a service serial interface for manufacturing, debug, recovery, and controlled firmware update.

Item	Specification
Electrical level	3.3 V logic-level UART
Default baud rate	115200 baud
Frame format	8 data bits, no parity, 1 stop bit (8N1)
Factory / debug / recovery use	Manufacturing programming, debug access, and recovery
Field update preference	Management bus is the preferred path for field firmware update
Recovery path	Service serial bootloader provides the recovery update path
Security	Firmware image authentication is required before programming
Safety	Firmware update is blocked unless the module is placed in a maintenance state by the chassis manager

6.5 Telemetry and Status

The management controller provides the following telemetry and status, including branch-level and converter-section-level monitoring.

Monitored item	Provided
Input voltage	Yes
Input current	Yes
Input power	Yes
Branch A current / branch load status	Yes
Branch B current / branch load status	Yes
Branch balance status	Yes
+12 V_MAIN voltage	Yes
+12 V_MAIN current	Yes
+12 V_MAIN power	Yes
+12 V conversion section A status	Yes
+12 V conversion section B status	Yes
+3.3 V_AUX voltage	Yes
+3.3 V_AUX current	Yes
+3.3 V_AUX power	Yes
+3.3 V_AUX conversion section A status	Yes
+3.3 V_AUX conversion section B status	Yes
+12 V ORing status	Yes
+3.3 V_AUX ORing status	Yes
Input switch status	Yes
ENABLE* state	Yes
INHIBIT* state	Yes
Geographic address	Yes
Management-bus health	Yes
Runtime hours	Yes
Restart counter	Yes
Fault log	Yes

Table 6 — Telemetry and status provided over the management interface.

6.6 Temperature Sensor Allocation

The module provides six temperature sensors through the management interface, covering the input stage, both filtered branches, both output combining areas, and the card-edge thermal interface.

Sensor	Location	Purpose
TEMP1	Input protection / hot-swap / shunt area	Detect input-stage and measurement-path heating
TEMP2	Branch A filter and conversion area	Detect Branch A filter and conversion thermal margin
TEMP3	Branch B filter and conversion area	Detect Branch B filter and conversion thermal margin
TEMP4	+12 V output ORing / combining area	Detect +12 V_MAIN ORing thermal margin
TEMP5	+3.3 V_AUX output ORing / combining area	Detect +3.3 V_AUX ORing thermal margin
TEMP6	Card-edge / wedge-lock thermal interface	Estimate chassis thermal interface and operating condition

Table 7 — Temperature sensor allocation (six sensors).

6.7 Required Fault Events

The following fault events are detected, reported, and logged, including branch-level and converter-section-level faults.

Fault event	Module response
Input undervoltage	Report; inhibit or shut down outputs if the operating limit is exceeded
Input overvoltage	Report; protect the module and shut down if required
Input overcurrent	Report; current-limit or shut down the input path
Branch A overcurrent	Report; current-limit or isolate the affected branch
Branch B overcurrent	Report; current-limit or isolate the affected branch
Branch imbalance	Report; rebalance or derate as required
Branch filter overtemperature	Report; derate or shut down the affected branch
+12 V conversion section imbalance	Report; rebalance or isolate the affected section
+3.3 V_AUX conversion section imbalance	Report; rebalance or isolate the affected section
+12 V overcurrent	Report; current-limit or shut down +12 V_MAIN
+3.3 V_AUX overcurrent	Report; current-limit or shut down +3.3 V_AUX
Output overvoltage	Report; shut down the affected rail
Output undervoltage	Report; indicate rail not valid
Output short circuit	Report; protected shutdown of the affected rail
ORing fault	Report; isolate the affected rail path
Reverse-current event	Report; block reverse current and isolate the affected path
Overtemperature	Report; derate or shut down depending on threshold
Management-bus fault	Report; preserve safe power state
Controller watchdog event	Watchdog reset; preserve safe power state

7. FDIR — Fault Detection, Isolation, and Recovery

7.1 FDIR Architecture

FDIR operates locally. Local hardware protection handles fast electrical faults independently of firmware. Firmware supervision handles thresholding, debouncing, event generation, retry policy, latching policy, and logging. The module preserves a safe power state even if management communication is interrupted.

Layer	Function
Local hardware fast protection	Protects against surge, reverse input, short circuit, and output overvoltage
Hardware status capture	Presents input-switch, branch, converter-section, ORing, and rail-good status to the controller
Firmware supervision	Thresholding, debouncing, event generation, retry policy, latching policy, and logging
Management reporting	Sends sensor events, FAIL* state, and logs to the chassis manager over IPMB-A and IPMB-B
Recovery policy	Retry, isolate, derate, latch off, or wait for command

7.2 FDIR Flow

The module detects a condition, qualifies and classifies it, isolates the affected path, enters a safe state and reports, records the event in nonvolatile memory, and applies the recovery decision.

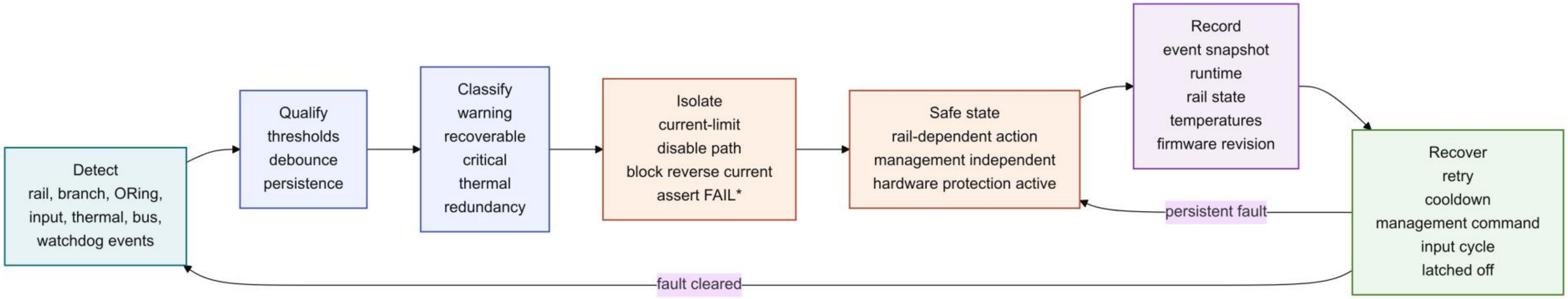

Figure 5 — FDIR detect-classify-isolate-recover flow.

7.3 Fault Classes and Recovery Policy

Fault class	Examples	Action	Recovery
Warning	Near-limit temperature, high load, input near limit	Report; continue operation	Clear after hysteresis
Recoverable	Transient overcurrent, transient undervoltage, branch imbalance	Disable or current-limit the affected path	Limited automatic retry
Critical	Output overvoltage, persistent short circuit	Shut down the affected rail and assert FAIL*	Latched until clear or input cycle
Thermal critical	Overtemperature beyond shutdown threshold	Derate or shut down	Restart after cooldown
Redundancy	ORing abnormality, reverse-current event	Isolate the affected path	Management-guided recovery
Management	Bus failure, controller watchdog event	Preserve safe power state	Watchdog or command recovery

7.4 Nonvolatile Fault Memory

The module records event snapshots in nonvolatile fault memory. Each record captures the event, runtime, rail conditions, branch status, temperatures, restart counter, and firmware revision, supporting FDIR evidence capture and field diagnostics.

Stored record	Content
Fault class and source	Warning, recoverable, critical, thermal, redundancy, or management; and the originating sensor, branch, section, rail, control pin, or bus
Runtime counter at fault	Accumulated runtime when the event occurred
Input snapshot	Input voltage and current at the time of the event
Output snapshot	Rail voltage and current at the time of the event
Branch status	Branch A and Branch B load and balance status
Temperature snapshot	All six temperature-sensor values
Restart counter	Number of restart attempts since last clear
Firmware revision	Management firmware revision in use during the event

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8. Grounding and Isolation

8.1 Interface Domains

The module uses isolated input-to-output conversion. The following are distinct interface domains and shall be treated separately unless the system grounding plan intentionally bonds them.

Domain	Description
Input return	Return for the 16–36 VDC input source
Output power return	Return for +12 V_MAIN and +3.3 V_AUX outputs
Signal return	Reference for management and control signals
Chassis / frame	Mechanical frame, shield, and EMI reference

8.2 Isolation and Bonding Ratings

Interface	Specification
Input return to output power return	500 VDC minimum isolation withstand
Input return to chassis	500 VDC minimum isolation withstand
Output power return to chassis	500 VDC minimum isolation withstand
Signal return to chassis	100 VDC minimum withstand unless tied by system profile
Insulation resistance	≥10 MΩ at 500 VDC between isolated domains
Chassis bond	≤10 mΩ from module frame / conduction edge to chassis
Interface ESD	±8 kV contact and ±15 kV air

8.3 Grounding Rules

- SIGNAL_RETURN and CHASSIS shall not be used as load-current returns.
- POWER_RETURN shall be sized for 65 A combined output-return current.
- Treat input return, output return, signal return, and chassis as separate domains unless the system grounding plan intentionally bonds them.
- Route remote sense as a Kelvin pair with SENSE_RETURN and protect it against open-circuit conditions.
- Use isolated or differential test equipment when measuring across the input-to-output isolation barrier.

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9. Mechanical and Thermal Integration

9.1 Mechanical Interface

Parameter	Specification
Form factor	3U VPX power module
Module pitch	1.0 inch VPX power-module envelope
Envelope	3.94 in W × 6.63 in L × 0.97 in H maximum
Mass	1.8 lb typical, 2.0 lb maximum
Retention	Wedge-lock retained

9.2 Thermal Interface

The module is conduction cooled through the card edge and wedge-lock path. The chassis shall maintain the card-edge temperature at or below +85 °C at rated load. No airflow is required for rated operation when the chassis conduction path meets the card-edge limit.

Parameter	Specification
Cooling method	Conduction cooled through card edge and wedge-lock path
Card-edge full-load temperature	+85 °C maximum
Airflow	Not required when the chassis conduction path meets the card-edge limit

9.3 Mechanical Drawings

The following mechanical drawing set is provided with the product data package.

Drawing	Content	Integration use
Outline drawing	Overall module envelope, connector datum, wedge-lock locations, card-edge references, keep-out zones	Chassis envelope and slot fit
Connector interface drawing	Connector type, datum, mating depth, keying position, pin-field orientation	Backplane and slot compatibility
Thermal interface drawing	Card-edge thermal surfaces, wedge-lock contact surfaces, thermal-pad zones	Chassis thermal design
Mass properties drawing	Mass, centre of gravity, insertion/extraction envelope	Shock, vibration, and handling analysis

9.4 Mechanical Integration Requirements

Item	Requirement
Slot pitch	1.0 inch VPX power slot
Maximum module width	3.94 in
Maximum module length	6.63 in
Maximum module height	0.97 in
Maximum mass	2.0 lb
Typical mass	1.8 lb
Card-edge thermal contact	Both conduction edges fully engaged
Wedge-lock engagement	Fully seated before applying rated load
Connector alignment	Connector mates without side-load or forced insertion

10. Environmental Specification

10.1 Temperature

Parameter	Specification
Operating temperature	-40 °C to +85 °C card-edge
Startup temperature	-46 °C minimum
Storage temperature	-55 °C to +105 °C

10.2 Altitude and Pressure

Parameter	Specification
Operating altitude	-1,500 ft to +70,000 ft equivalent
Vacuum operation	$\leq 1 \times 10^{-5}$ torr with conduction cooling

Vacuum operation requires a valid chassis conduction-cooling path because convective cooling is not available in vacuum.

10.3 Shock and Vibration

Parameter	Specification
Mechanical shock	40 g, 11 ms half-sine, 18 shocks
Random vibration	0.1 g^2/Hz, 1 hour per axis

10.4 Humidity, Corrosion, and ESD

Parameter	Specification
Humidity	95% RH, non-condensing
Salt fog / corrosion	SL1 / ASTM G85 Annex A4 style exposure
Interface ESD	±8 kV contact and ±15 kV air
Coating	Conformal coating on the populated assembly

11. Handling and Safety

Safety notice
Treat conduction surfaces as hot when the card-edge temperature exceeds +60 °C. Observe ESD precautions at all times and do not exceed the input or output limits stated below.

Item	Numeric requirement / limit
ESD handling	Use a grounded wrist strap and ESD-safe surface; interface ESD rating ±8 kV contact and ±15 kV air
Input voltage limit	Do not exceed 36 VDC continuous input
Input current provision	Chassis input path shall support 45 A per module at low-line operation
Output load limit	Do not exceed +12 V at 46 A or +3.3 V_AUX at 15 A
Surface temperature	Treat conduction surfaces as hot above +60 °C card-edge temperature
Maximum card-edge operation	+85 °C
Cooldown before handling	Allow 5 minutes after high-load operation before bare-hand handling
External +12 V capacitance	Up to 5 mF system-added capacitance
External +3.3 V_AUX capacitance	Up to 10 mF system-added capacitance
Firmware update safety	Do not update firmware while the module is the only active power source for mission loads

12. Verification

The module is verified against the following conditions and acceptance criteria.

Test area	Numeric condition	Acceptance criterion
Connector continuity	100% of pin-map contacts	All contacts match this guide; no shorts to no-connect contacts
Input range	16 V, 28 V, and 36 V input	Rails start, regulate, and report valid telemetry
Low-line full load	16 V input, +12 V at 46 A, +3.3 V at 15 A	Input current ≤45 A, no shutdown
Branch balance	Full load at 16 V	Each filtered branch below the 22 A rating
Output regulation	No load, half load, full load	Within rail tolerance
Output ORing	Backfeed with peer rail active	Reverse current blocked
Short circuit	+12 V and +3.3 V_AUX rail shorts	Protected response, fault logged, no damage
Thermal	+85 °C card edge, full load	No thermal shutdown, all six sensors valid
Management buses	Poll all telemetry on IPMB-A and IPMB-B	All required items readable on both buses
FDIR injection	UV, OV, OC, OT, branch, ORing, and bus faults	Correct event, FAIL*, log, and recovery action
Nonvolatile fault memory	Fault snapshot write and read-back	All required fields retained
Service UART	115200 8N1 recovery update	Authenticated recovery path succeeds
ESD	±8 kV contact, ±15 kV air	No permanent damage; any upset self-recovers and is logged
Random vibration	0.1 g^2/Hz, 1 hour per axis	No rail dropout >10 μs, no management reset
Mechanical shock	40 g, 11 ms half-sine, 18 shocks	No mechanical damage, post-test electrical pass
Altitude	-1,500 ft to +70,000 ft equivalent	No arcing, rail regulation maintained
Vacuum operation	$\leq 1 \times 10^{-5}$ torr with conduction cooling	Rail regulation and temperatures within limits
Temperature cycling	500 cycles, -55 °C to +105 °C	No structural damage, post-test electrical pass
Humidity	95% RH, non-condensing	No corrosion-induced malfunction

Table 8 — Verification conditions and acceptance criteria.

13. Getting Started and Installation

13.1 Pre-Installation Checks

1. Confirm that the chassis slot is a compatible 3U VPX power-supply slot.
2. Confirm that the backplane pin allocation matches the CAVU PSU-Polar-3U SOSA-aligned pin map in Section 4.
3. Confirm that the system input source is within 16–36 VDC continuous limits and supports 45 A per module.
4. Confirm that the expected +12 V_MAIN and +3.3 V_AUX loads do not exceed the rated current limits.
5. Confirm that the chassis provides an adequate conduction-cooling path to the card edge.
6. Confirm that each installed module has a unique geographic address.

13.2 Installation

1. Remove input power from the chassis before insertion unless the chassis is designed for live insertion of VPX power modules.
2. Inspect the connector, guide rails, wedge locks, and thermal interfaces.
3. Insert the module fully into the assigned power-supply slot.
4. Secure the wedge locks according to the chassis torque procedure.
5. Apply input power and monitor the management interface for module presence, sensor validity, and rail status.

13.3 Shutdown

The module is shut down by deasserting ENABLE*, asserting INHIBIT* for the main rail, removing input power, or issuing a supported management command. The preferred sequence is to remove or inhibit the payload load before removing input power.

14. Troubleshooting

Symptom	Likely cause	Recommended action
Module not visible on either management bus	Geographic address conflict or missing bus pull-ups	Verify unique geographic address and backplane bus pull-ups
+12 V_MAIN remains off while +3.3 V_AUX is on	INHIBIT* asserted or AUX-only state commanded	Release INHIBIT* and confirm ENABLE* asserted
FAIL* asserted at power-up	Input out of range or detected fault	Check input voltage 16–36 VDC and review the fault log
Branch imbalance reported	Asymmetric branch loading or thermal condition	Review branch telemetry and confirm chassis thermal path
Thermal warning at moderate load	Card-edge thermal path not fully engaged	Verify wedge-lock preload and clean conduction interfaces
Poor output regulation under load	Remote sense open or mis-routed	Confirm Kelvin sense routing and SENSE_RETURN integrity
Firmware update rejected	Image authentication failed or module not in maintenance state	Use an authenticated image and place the module in maintenance state

15. Related Documents

Reference	Description
VITA 46.0	VPX baseline standard
VITA 46.11	System management on VPX
VITA 48.x	VPX REDI mechanical standards
VITA 62	VPX power supply module interface
VITA 65 / OpenVPX	OpenVPX system architecture
SOSA Technical Standard	Sensor Open Systems Architecture
MIL-STD-704	Aircraft electric power characteristics
MIL-STD-461	Electromagnetic interference requirements
MIL-STD-810	Environmental engineering considerations and laboratory tests
MIL-STD-1275	Characteristics of 28 VDC input power (where applicable)
RTCA/DO-160	Environmental conditions and test procedures for airborne equipment (where applicable)
CAVU connector interface drawing	Authoritative connector and pin-field definition
CAVU mechanical outline drawing	Module envelope and mechanical interface
CAVU thermal interface drawing	Card-edge and wedge-lock thermal interface
CAVU management interface ICD	Management sensor map, command set, and event definitions