STD. OBC-HYPER-POLAR

User Manual & ICD

Electrical, Mechanical & Software Interfaces

CAVU
AEROSPACE UK

Document Specification

Field	Value
Document	CAVU-OBC-HYPER-UM
Title	Electrical, Mechanical & Software Interfaces
Product	OBC-HYPER-POLAR
Version	03
Status	Released
Date	29 May 2026
Written by	H.S
Verified by	A.A
Approved by	C.E
Company	CAVU Aerospace
Address	12 Scion House, Stirling University Innovation Park, Stirling FK9 4NF, UK
Classification	Customer deliverable

Document Change Record

Version	Date	Author	Description
01	May 2026	A.A.	Initial release — CAVU-OBC-HYPER-UM

Table of Contents

Abbreviations

AGND	Analogue ground
ADC	Analogue-to-Digital Converter
AMP	Asymmetric multiprocessing
BSP	Board Support Package
CAN	Controller Area Network
DDR4	Double Data Rate 4 SDRAM
DMIPS	Dhrystone Million Instructions per Second
ECC	Error-Correcting Code
ECSS	European Cooperation for Space Standardization
eMMC	embedded MultiMediaCard (managed NAND)
EMC	Electromagnetic Compatibility
ESD	Electrostatic Discharge
FM	Flight Model
FDIR	Failure Detection, Isolation and Recovery
FPGA	Field-Programmable Gate Array
GbE	Gigabit Ethernet
GPIO	General-Purpose Input/Output
HSS	Hart Software Services — PolarFire SoC supervisor running on the E51 monitor core
I^2C	Inter-Integrated Circuit
ICD	Interface Control Document
JTAG	Joint Test Action Group (IEEE 1149.1)
LCL	Latch-up Current Limiter
LPDDR4	Low-Power Double Data Rate 4 SDRAM
LVDS	Low-Voltage Differential Signalling
MRAM	Magneto-resistive Random-Access Memory
MSS	Microprocessor Subsystem (PolarFire SoC integrated RISC-V complex)
NC	No Connect (pin permanently unconnected on the PCB)
OBC	On-Board Computer
OVP	Over-Voltage Protection
PHY	Physical-layer transceiver
pSLC	pseudo-Single-Level-Cell (eMMC managed-NAND operating mode)
QM	Qualification Model

QSPI	Quad Serial Peripheral Interface
RISC-V	Reduced Instruction Set Computer V (open ISA)
RS-232	Recommended Standard 232 — serial, single-ended
RS-422	Recommended Standard 422 — serial, differential, point-to-point
RS-485	Recommended Standard 485 — serial, differential, multi-drop
RTC	Real-Time Clock
SBI	Supervisor Binary Interface (RISC-V)
SBC	Single-Board Computer
SECDED	Single-Error-Correct Double-Error-Detect (ECC scheme)
SEU	Single-Event Upset
SGMII	Serial Gigabit Media-Independent Interface
SMP	Symmetric multiprocessing
SoC	System-on-Chip
SPI	Serial Peripheral Interface
SpW	SpaceWire (ECSS-E-ST-50-12C)
UART	Universal Asynchronous Receiver/Transmitter
UVLO	Under-Voltage Lock-Out
USB	Universal Serial Bus
WDT	Watchdog Timer
XCVR	SerDes Transceiver
ZeroFIT	Microchip designation for zero inherent failure-in-time (flash-based PolarFire fabric)

1. Introduction

1.1 Purpose and Scope

This document defines the electrical, mechanical and software interfaces of the CAVU OBC HYPER-POLAR on-board computer.

This manual is intended for system integration engineers responsible for incorporating the OBC HYPER-POLAR into a spacecraft, instrument or ground-support harness, and for software engineers responsible for bring-up, image management and application development. It provides every piece of information necessary to design, fabricate and verify the interface cables, the mounting arrangement, and the bring-up and software-update procedures.

Internal circuit design is outside the scope of this document. For supplementary technical content the following CAVU documents apply:

- CAVU-OBC-HYPER-POLAR-ICD_v1.0 — Interface control specification.
- CAVU-OBC-HYPER-POLAR-WDM_v1.0 — Watchdog and System Monitoring document (see §A.1).
- CAVU-OBC-HYPER-POLAR-RAR_v1.0 — Reliability Analysis Report.
- CAVU-OBC-HYPER-POLAR-FMEA_v2.0 — Failure Modes, Effects & Criticality Analysis.
- CAVU-OBC-HYPER-POLAR-CIL_v2.0 — Critical Items List.

1.2 How to Use This Guide

The recommended reading path depends on the reader's immediate task:

- **For first-time integration:** Read Chapter 1 to understand the product context. Then review Chapter 2 to familiarise yourself with the hardware architecture, system specifications, and connector inventory. Chapter 3 contains the detail required to design each interface cable. Chapters 4 and 5 cover environmental qualification and bring-up.
- **For connector pin-out reference:** Go directly to the relevant sub-section of Chapter 3. Each interface section is self-contained and includes a pin table with cable colour codes, the connector part number, electrical characteristics, and a figure reference.
- **For mechanical integration:** Section 2.7 lists mass properties; §4.3 gives mechanical specifications and the dimensional drawing; §2.8 lists every external connector.
- **For system bring-up:** Chapter 5 covers initial power-on, the HSS supervisor, image management and software development tooling.

Conventions used in this document:

- **WARNING:** A condition that, if not avoided, could damage the OBC HYPER-POLAR or the host system, or invalidate warranty.
- **CAUTION:** A condition that could result in degraded performance or minor damage.
- **NOTE:** Supplementary information, clarification or cross-reference.

Pin tables use the following conventions:

- Signal names follow the CAVU OBC HYPER-POLAR net-naming convention.
- "GND" is signal/return ground. "AGND" is analogue ground, star-connected to GND inside the enclosure.
- "NC" indicates a pin permanently not connected on the PCB. Do not connect to NC pins in the mating harness.
- Cable colour codes are CAVU's recommended convention for cable harnesses supplied with the unit; mating harnesses procured by the customer may use any colour scheme provided the signal mapping is preserved.

1.3 Platform Overview

OBC HYPER-POLAR is built around the Microchip PolarFire SoC FPGA, which provides a hardened RISC-V Microprocessor Subsystem (MSS — four U54 application cores and one E51 monitor core, > 4 000 DMIPS total) and a flash-based FPGA fabric on a single die. The flash-based fabric is the central feature of the platform: it is inherently non-volatile at power-up and exhibits zero inherent failure-in-time (ZeroFIT) with respect to single-event upsets, so it requires no external configuration storage and no in-orbit scrubbing for the configuration cells. The fabric is live the instant the device is powered.

The OBC HYPER-POLAR is delivered as a complete, enclosed flight-ready system. Aluminium enclosure provides mechanical rigidity, EMC shielding and thermal spreading. All external interfaces are presented through rugged Micro-D family connectors (MIL-DTL-83513) and a single Glenair GMPM2 power connector.

Figure 1: OBC Front View

2. System Overview

2.1 Hardware Architecture

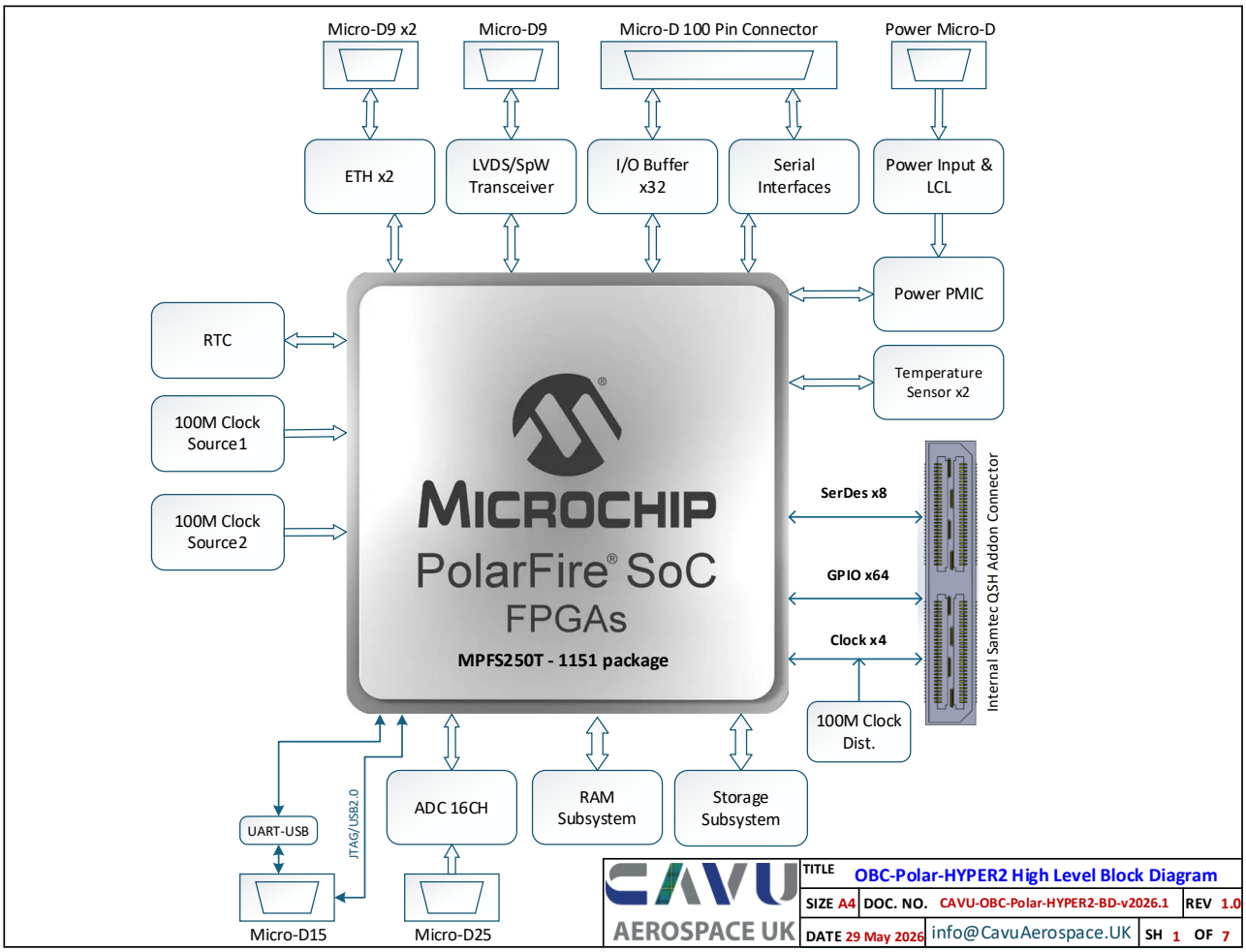

Figure 2: OBC-HYPER-POLAR High Level Block Diagram

The hardware architecture is centred on the PolarFire SoC, which acts simultaneously as the main processor complex and the programmable-logic fabric. The remainder of the OBC consists of:

- A working-memory tier — DDR4 with SECDED ECC on the fabric, LPDDR4 on the MSS.
- A persistent-storage tier — two pSLC-configured eMMC devices, two QSPI NOR Flash banks, and one SPI MRAM.
- A serial-interfaces tier — four CAN, four RS-422 (full-duplex), four RS-485, four RS-232, and one I^2C, all presented through dedicated PHYs onto the front-panel 100-pin Micro-D Serial I/O connector.
- A high-bandwidth tier — two Gigabit Ethernet ports (LAN1, LAN2) on the main board, two LVDS / SpaceWire links and the high-speed Samtec QSH-060 expansion connector.
- An acquisition tier — a 16-channel, 16-bit simultaneous-sampling AD7616 ADC on the back-panel 25-pin Micro-D.
- A debug and programming tier — JTAG (FlashPro5/6), PolarFire native USB 2.0, dual USB-to-UART debug console (CP2105), all aggregated on the back-panel 15-pin Micro-D and broken out by the CAVU-HYPER-POLAR-DBG debug adapter card.
- A power tier — wide-input LCL stage feeding redundant on-board DC-DC conversion; all internal rail generation is internal to the unit.

2.1.1 PolarFire SoC

The PolarFire SoC integrates two tightly-coupled subsystems on a single die: the hardened RISC-V MSS and the programmable FPGA fabric. The MSS provides four U54 application cores (RV64GC, dual-issue, in-order), one E51 monitor core (RV64IMAC, single-issue, in-order, dedicated supervisor), hard peripheral controllers (Ethernet MAC, CAN, UART, SPI, I^2C, USB) and a high-bandwidth AXI interconnect. The FPGA fabric provides user-programmable logic, DSP blocks, on-chip SRAM and the SerDes transceivers used for high-speed off-chip links.

2.1.2 Working Memory

DDR4 (fabric working memory). A 72-bit-wide DDR4 SDRAM array is connected to the FPGA fabric memory controller. The array provides 8 Gbyte of user-visible storage with full SECDED ECC: the underlying physical array is 64 Gbit data + 8 Gbit ECC (9 Gbyte physical) running 72-bit wide. Any single-bit error in a 64-bit word is corrected transparently; any double-bit error is detected and flagged.

LPDDR4 (MSS working memory). A 32-bit-wide LPDDR4 SDRAM device is connected directly to the MSS memory controller. Total capacity is 4 Gbyte (32 Gbit). LPDDR4 provides low-latency, lower-power working memory for the application cores and the operating system.

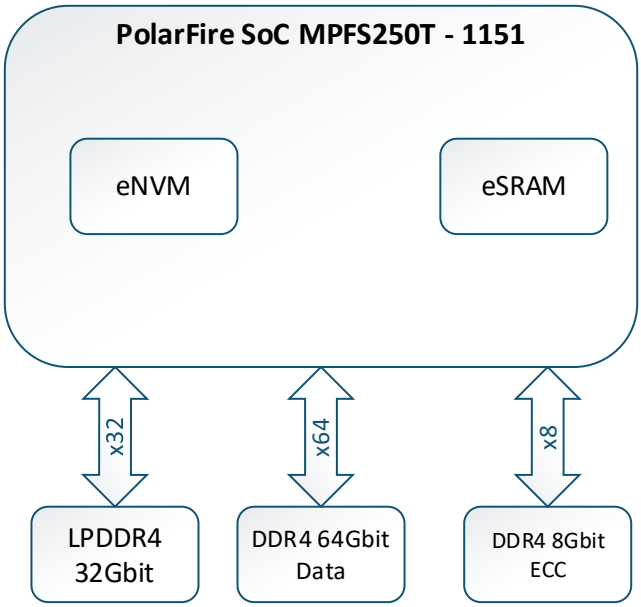

Figure 3: OBC-HYPER-POLAR Memories

2.1.3 Persistent Storage (eMMC, QSPI, MRAM)

Dual eMMC (mass storage, pSLC). Two independent eMMC devices provide non-volatile mass storage. The factory default configuration runs each device in **pseudo-SLC (pSLC) mode:** each cell stores a single bit instead of the native multi-level encoding. In this mode the user-visible capacity of each eMMC is approximately 80 Gbyte. pSLC mode is selected because it substantially improves data retention, write endurance and error margin compared with native TLC/QLC operation, which is critical for unattended space and aerospace operation.

> **NOTE** In pSLC mode the program/erase endurance per block is typically 50 000 – 100 000 cycles (versus 1 000 – 3 000 cycles in native TLC), data-retention margin is significantly improved, and

> read disturb sensitivity is reduced. CAVU can configure full-capacity non-pSLC operation on request for missions where total volume is more important than write endurance.

eMMC-A is connected to the MSS SDIO/eMMC host controller; eMMC-B is connected to the fabric SDIO interface. The two devices are managed independently, supporting redundant-OS, dual-payload, or paired storage configurations.

Dual QSPI NOR Flash. Two 512 Mbit QSPI NOR Flash devices are present on the main board. They store the HSS payload (signed binary containing OpenSBI, U-Boot, optional fabric design overlay). The two banks form the primary boot path of the HSS supervisor (see §5.2): QSPI-A is the primary payload, QSPI-B is the redundant payload. **Important:** the PolarFire fabric itself is flash-based and is loaded internally from the SoC die; it is not loaded from these external QSPI Flash devices.

SPI MRAM. A 4 Mbit SPI MRAM device provides radiation-hard, zero-write-wear non-volatile storage for critical state: boot pointer, image-validity counters, FDIR event log, and the rescue payload pointer used by HSS at boot fallback (see §5.2).

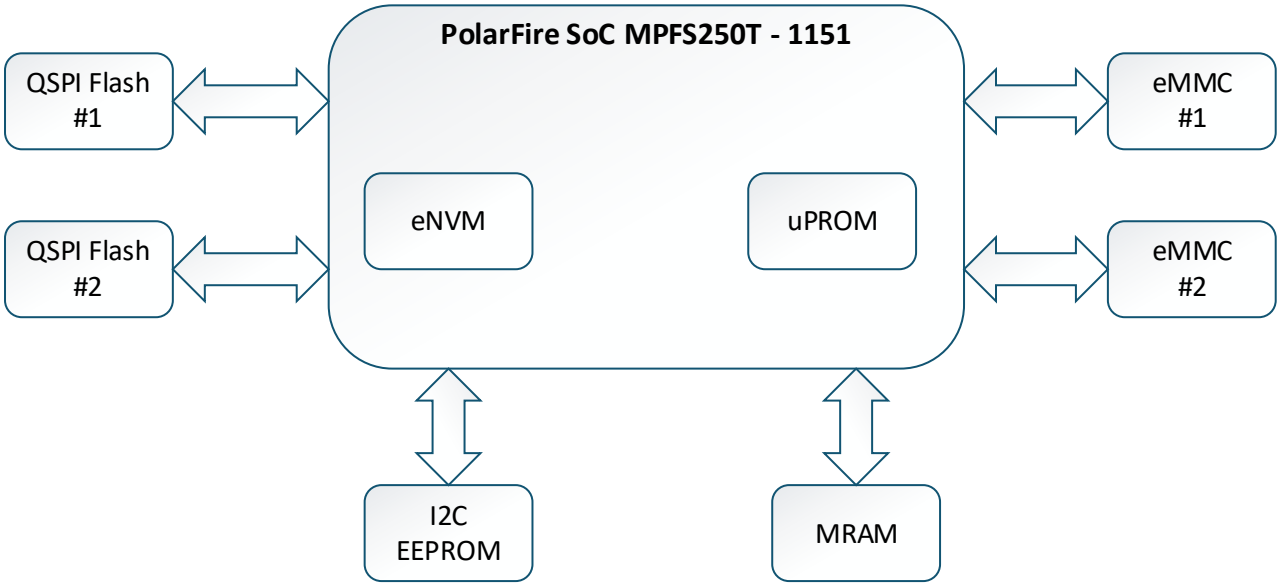

Figure 4: OBC-HYPER-POLAR Non-Volatile Storages

2.1.4 Analogue Acquisition

A 16-channel, 16-bit simultaneous-sampling AD7616 ADC is mounted on the main board. All 16 input channels and the 3.3 V / 5 V reference outputs are routed via internal cable to the back-panel 25-pin Micro-D ADC connector. The input range is factory-selectable as ±5 V or ±10 V (default: ±10 V). The ADC is interfaced to the FPGA fabric over SPI.

2.1.5 Gigabit Ethernet

Two Gigabit Ethernet channels (LAN1, LAN2) are implemented on the main board using SGMII PHYs connected to the PolarFire SoC hard Ethernet MACs. They use a transformer-less, capacitive-coupled 1000BASE-T physical layer and are routed to 9-pin Micro-D connectors on the front panel.

2.1.6 Serial Communication PHYs

Dedicated transceiver ICs implement the RS-422, RS-232, RS-485 and CAN physical layers. Two of the four CAN channels are driven by PolarFire SoC hard CAN controllers (MSS); the other two are implemented in the FPGA fabric. All serial signals are aggregated on the 100-pin Micro-D Serial I/O connector on the front panel.

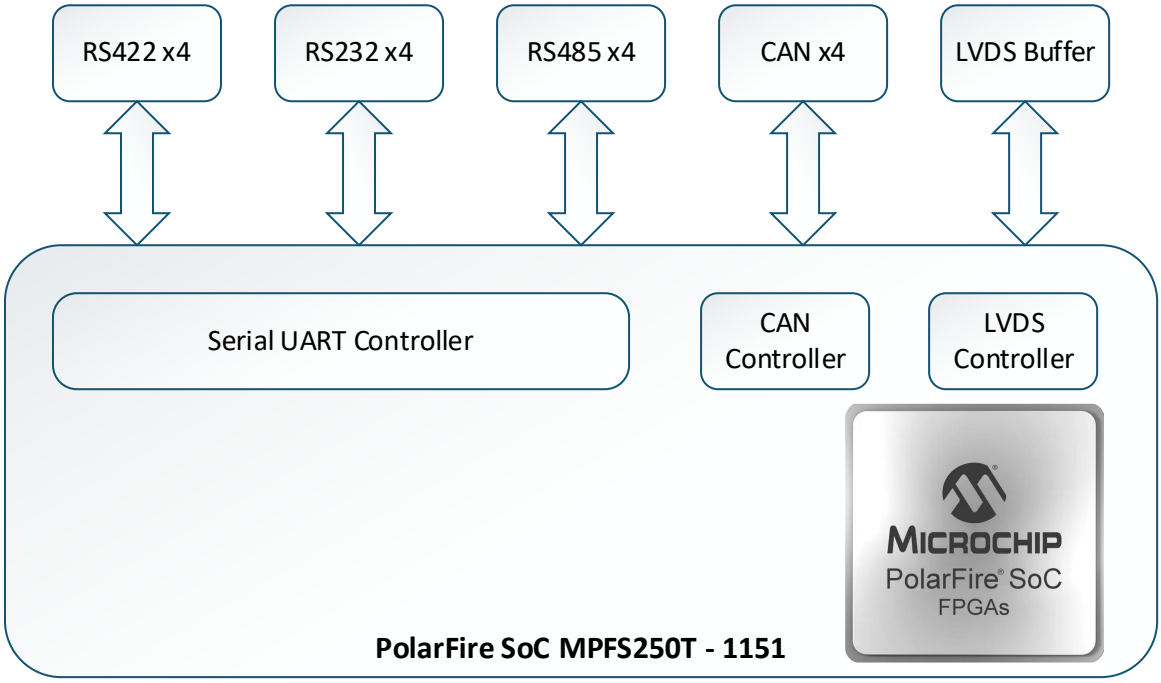

Figure 5: OBC-HYPER-POLAR Serial Interfaces

2.1.7 GPIO

Thirty-two general-purpose I/O signals are buffered through external buffer ICs. They are organised in four banks of eight signals each, with bank-level direction control: each bank is set as either all-input or all-output independently of the other banks. A further eight Direct-IO signals are connected directly to PolarFire SoC fabric I/O pins (no external buffer). The dedicated I^2C bus (SCL3.3, SDA3.3) is also present on the 100-pin Serial I/O connector.

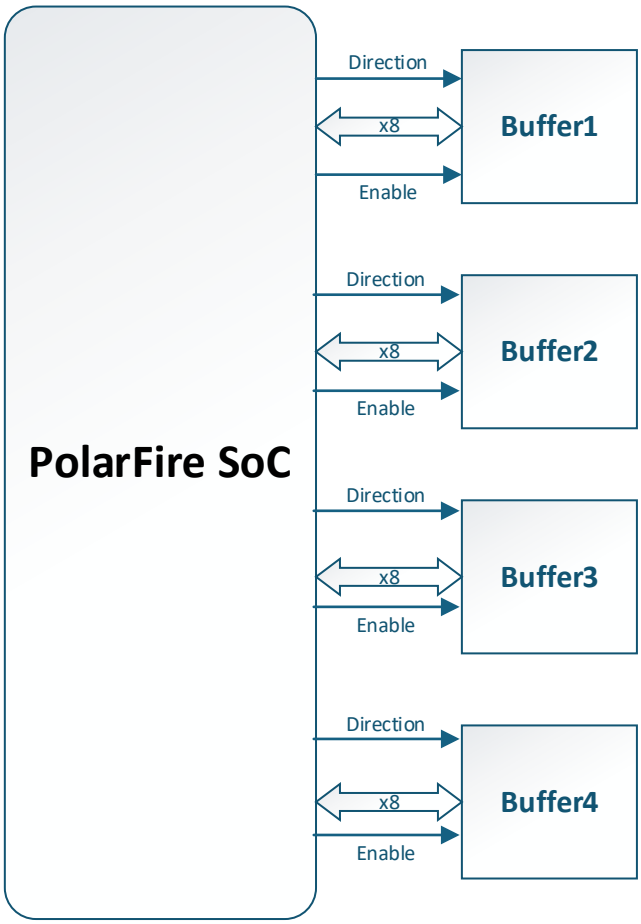

Figure 6: OBC GPIO Buffers

2.1.8 LVDS / SpaceWire

Two LVDS transmit/receive pairs (TX1/RX1 and TX2/RX2) are routed to the 9-pin Micro-D LVDS/SpaceWire connector on the front panel. The signal levels, differential impedance and connector pinout are compatible with ECSS-E-ST-50-12C SpaceWire. The link-layer protocol is implemented in the FPGA fabric.

2.1.9 USB, JTAG and Debug

The PolarFire SoC native USB 2.0 interface, two UART debug channels (via CP2105 USB-to-UART bridge) and the JTAG signals for FlashPro5/6 programming are aggregated on the back-panel 15-pin Micro-D JTAG/USB/Debug connector. The supplied CAVU-HYPER-POLAR-DBG debug adapter card breaks them out to standard USB and 2×5 FlashPro headers for development use (see §3.7).

2.1.10 Power Input Stage

The input power stage accepts a wide-range unregulated DC supply at the GMPM2 2-pin connector on the front panel. The first stage after the connector is a Latch-up Current Limiter (LCL): an active protection element that combines reverse-polarity protection, in-rush current limiting, over-current limiting with foldback, over-voltage protection (OVP) and under-voltage lock-out (UVLO) into a single coordinated function. The LCL acts as the primary defence against upstream faults, single-event transients and harness anomalies, and supports automatic retry behaviour for transient over-current events.

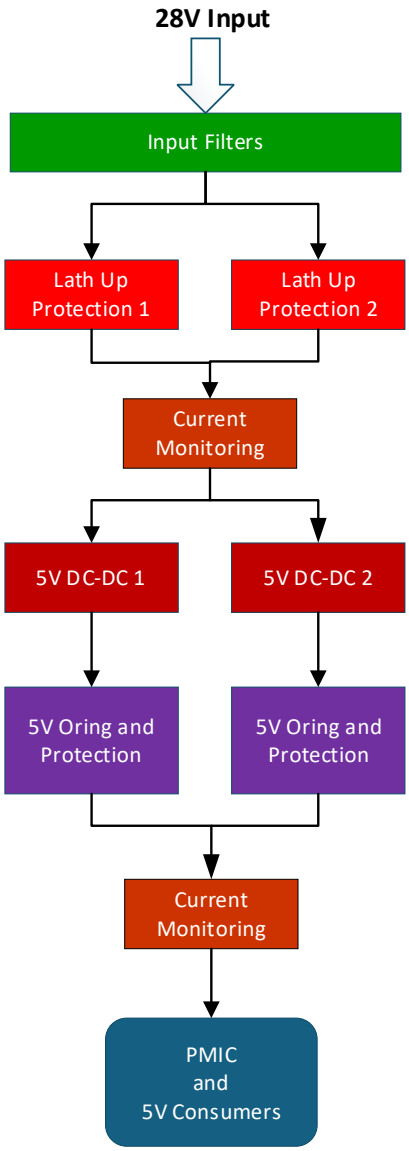

Figure 7: OBC Power Path

The factory-default OVP and UVLO thresholds are hardware-set on the LCL stage (see §3.1) and are not under software control during nominal operation. Downstream of the LCL, redundant on-board DC-DC conversion produces the regulated rails required by the PolarFire SoC, memory, PHYs and peripheral ICs; the internal regulator architecture is not user-configurable and is not described in this manual.

2.1.11 Watchdog and System Monitoring

System health, hardware watchdog architecture, FDIR rules, autonomous recovery and on-board housekeeping channels are documented in a dedicated reference document supplied with the OBC HYPER-POLAR delivery package:

Reference: CAVU-OBC-HYPER-POLAR-WDM_v1.0 — Watchdog and System Monitoring.

That document is the authoritative reference for the supervisor-side watchdog logic, the heartbeat protocol between the E51 monitor core and the U54 application cores, the FDIR event-log format, the on-orbit telemetry channels, and the safe-mode behaviour. It is not duplicated in this manual.

2.2 Key Features Summary

- Microchip PolarFire SoC FPGA — three available variants (see §2.5).
- RISC-V MSS: 4× U54 application cores + 1× E51 monitor core; > 4 000 DMIPS combined.
- Flash-based FPGA fabric — ZeroFIT SEU immunity; live at power-up; no external configuration storage required.
- DDR4 SDRAM (fabric): 72-bit wide with SECDED ECC; 8 Gbyte user-visible (9 Gbyte physical).
- LPDDR4 SDRAM (MSS): 32-bit wide; 4 Gbyte.
- Dual eMMC mass storage: ~80 Gbyte each in pSLC mode (factory default).
- Dual 512 Mbit QSPI NOR Flash — primary and redundant HSS payload banks.
- 4 Mbit SPI MRAM — radiation-hard non-volatile state, rescue payload pointer, FDIR log.
- 4× CAN (2× MSS hard controllers, 2× fabric); 4× RS-422 full-duplex; 4× RS-232; 4× RS-485; 1× I^2C.
- 32× buffered GPIO in 4 banks of 8 (per-bank direction control); 8× Direct-IO (direct to fabric pins).
- 2× LVDS / SpaceWire pairs (ECSS-E-ST-50-12C compatible).
- 16-channel, 16-bit simultaneous-sampling AD7616 ADC; ±5 V / ±10 V factory-selectable.
- PolarFire native USB 2.0; USB-to-UART dual debug console (CP2105); JTAG (FlashPro5/6).
- 8× SerDes lanes (up to 12.7 Gbps each) routed to internal expansion connector.
- Wide-input LCL power stage; redundant on-board DC-DC conversion; hardware-configured OVP/UVLO (default 22–32 V, 28 V nominal).
- Aluminium enclosure 110 × 181 mm (with mounting tabs); height 21.9 mm.
- All I/O connectors: Micro-D (MIL-DTL-83513); power connector: Glenair GMPM2.

2.3 System Specifications

Table 3 consolidates the headline specifications of the OBC HYPER-POLAR in one place. Detailed per-interface electrical characteristics are tabulated in Chapter 3. Detailed environmental specifications are in Chapter 4.

Category	Parameter	Value
Processing	FPGA / SoC	Microchip PolarFire SoC (MPFS250T-1FCG1152I, MPFS460T-1FCG1152I, or MPFS460TS-FC1152M military-grade) — see §2.5
	RISC-V MSS	4× U54 (RV64GC) application cores + 1× E51 (RV64IMAC) monitor core
	Combined performance	> 4 000 DMIPS
	FPGA fabric	Flash-based, ZeroFIT, live at power-up
	Logic elements	254 k (MPFS250T) or 461 k (MPFS460T / MPFS460TS)
Working memory	DDR4 (fabric)	8 Gbyte user-visible, 9 Gbyte physical, 72-bit with SECDED ECC (64 Gbit data + 8 Gbit ECC)
	LPDDR4 (MSS)	4 Gbyte, 32 Gbit, 32-bit wide, direct to MSS controller
Persistent storage	eMMC × 2	Approximately 80 Gbyte each, pSLC mode (factory default); eMMC-A on MSS SDIO, eMMC-B on fabric SDIO
	QSPI NOR Flash × 2	512 Mbit each; primary/redundant HSS payload banks
	SPI MRAM	4 Mbit; non-volatile state, FDIR log, rescue pointer
Serial interfaces	CAN	4× channels (2× MSS hard controllers + 2× fabric), ISO 11898-2
	RS-422	4× channels, full-duplex (A=TX+, B=TX−, Y=RX+, Z=RX−), TIA/EIA-422
	RS-485	4× channels, TIA/EIA-485
	RS-232	4× channels, EIA/TIA-232
	I^2C	1× bus (SCL3.3 pin 6, SDA3.3 pin 31), 3.3 V; up to 400 kHz
Discrete I/O	Buffered GPIO	32 lines in 4 banks of 8; per-bank direction control
	Direct-IO	8 lines, direct to PolarFire fabric I/O (3.3 V)
High-speed I/O	LVDS / SpaceWire	2× pairs (TX/RX), ECSS-E-ST-50-12C compatible
	Gigabit Ethernet	2× ports (LAN1, LAN2), transformer-less capacitive-coupled 1000BASE-T
	SerDes lanes (expansion)	8× lanes up to 12.7 Gbps each, on internal Samtec QSH-060 expansion connector
Acquisition	ADC	16-channel, 16-bit, simultaneous-sampling AD7616; ±5 V / ±10 V factory-selectable
Debug	USB 2.0	PolarFire SoC native USB 2.0 (host or device)
	USB-to-UART	Dual virtual COM ports via CP2105 (HSS console + Linux console)
	JTAG	FlashPro5 / FlashPro6 compatible
Power	Input voltage (default)	22 V to 32 V DC (28 V nominal bus). Other ranges available on request — factory-configured.
	Input power consumption	Typical 3 W idle / 5 W nominal / ≤ 8 W peak (all PHYs active). See §3.1.5 and on-line estimator.
	Protection	LCL stage on input — OVP, UVLO, reverse polarity, in-rush limit; hardware-configured at factory.
Mechanical	Enclosure	Aluminium; 110 × 181 mm (with mounting tabs); height 21.9 mm
	Total mass	660 gr
	Mounting	4× 8-32 UNC, 4.5 mm through; 95 × 165 mm matrix
Environment	Operating temperature	−40 °C to +85 °C industrial (MPFS250T, MPFS460T-I); −55 °C to +125 °C military (MPFS460TS, on stock-dependent variant)
	Vibration / shock / EMC	Qualified at QM and FM (see Chapter 4)
Software	Supervisor	Hart Software Services (HSS) running on E51 monitor core, resident in eNVM
	OS support	Linux SMP (4× U54) by default; OpenSBI / U-Boot in the HSS payload; AMP and bare-metal supported
	Image redundancy	HSS payload fallback chain: QSPI-A → QSPI-B → eMMC-A → eMMC-B → MRAM rescue
	Watchdog & FDIR	See CAVU-OBC-HYPER-POLAR-WDM_v1.0

Table 3 — OBC HYPER-POLAR system specifications

2.4 Operating Modes

2.4.1 Software Execution Modes

OBC HYPER-POLAR supports two primary software execution environments:

- **Linux (SMP).** The four U54 application cores run a single SMP Linux kernel under U-Boot. This is the standard delivered configuration and provides a POSIX environment, file systems, IP networking, and standard middleware.
- **Bare-metal / RTOS (AMP).** One or more U54 cores run a bare-metal application or RTOS (FreeRTOS, Zephyr, RTEMS) for deterministic real-time work, while the remaining cores may simultaneously run Linux.

In every configuration the E51 monitor core runs HSS exclusively. The HSS is the resident supervisor and is described in §5.2.

2.4.2 Boot Sequence (Overview)

A high-level summary is given here; the operational detail is in §5.2.

At power-up:

1. The PolarFire SoC System Controller releases the MSS from reset. The flash-based FPGA fabric is live and configured at this point — there is no bitstream loading from external QSPI Flash at any time during the boot.
2. The MSS enters HSS code, which is resident in the SoC embedded non-volatile memory (eNVM) on the die.
3. HSS reads the active-bank pointer from MRAM, then walks the payload fallback chain — QSPI-A → QSPI-B → eMMC-A → eMMC-B → MRAM rescue — until a signed and verified payload is found.
4. HSS extracts the U54 payload, typically OpenSBI and U-Boot, into DDR4/LPDDR4 and releases the U54 cores.
5. OpenSBI provides the M-mode supervisor-binary interface; U-Boot loads and launches the Linux kernel (or other application image) from eMMC, QSPI or MRAM as configured.
6.

> **NOTE** The PolarFire SoC fabric is flash-based and is loaded internally from the die at power-up. Earlier revisions of this manual described an external QSPI bitstream load step — that description was incorrect for this platform and has been removed.

2.5 FPGA Variants

OBC HYPER-POLAR is available with one of three PolarFire SoC devices. The variant is specified at time of order and cannot be changed after PCB assembly.

Parameter	MPFS250T-1FCG1152I	MPFS460T-1FCG1152I	MPFS460TS-FC1152M
Logic elements	254 000	461 000	461 000
Screening / grade	Industrial (−40 to +100 °C)	Industrial (−40 to +100 °C)	Military (−55 to +125 °C)
FPGA Fabric µSRAM (kbit)	1 944	3 564	3 564
FPGA Fabric LSRAM (kbit)	16 128	32 256	32 256
DSP blocks (18×18 MAC)	336	672	672
RISC-V MSS	4× U54 + 1× E51	4× U54 + 1× E51	4× U54 + 1× E51
MSS performance	> 4 000 DMIPS	> 4 000 DMIPS	> 4 000 DMIPS
SerDes lanes	Up to 16 (8 to expansion)	Up to 16 (8 to expansion)	Up to 16 (8 to expansion)
Flash-based fabric (ZeroFIT)	Yes	Yes	Yes
Availability	Standard production	Standard production	Stock-dependent — contact CAVU

Table 4 — FPGA variant comparison

> **NOTE** The MPFS460TS-FC1152M military-grade device offers the extended −55 to +125 °C operating range and additional vendor screening. Its availability depends on stock and is offered on a build-to-order basis. Confirm availability with CAVU before configuration freeze.

2.6 Mechanical Outline

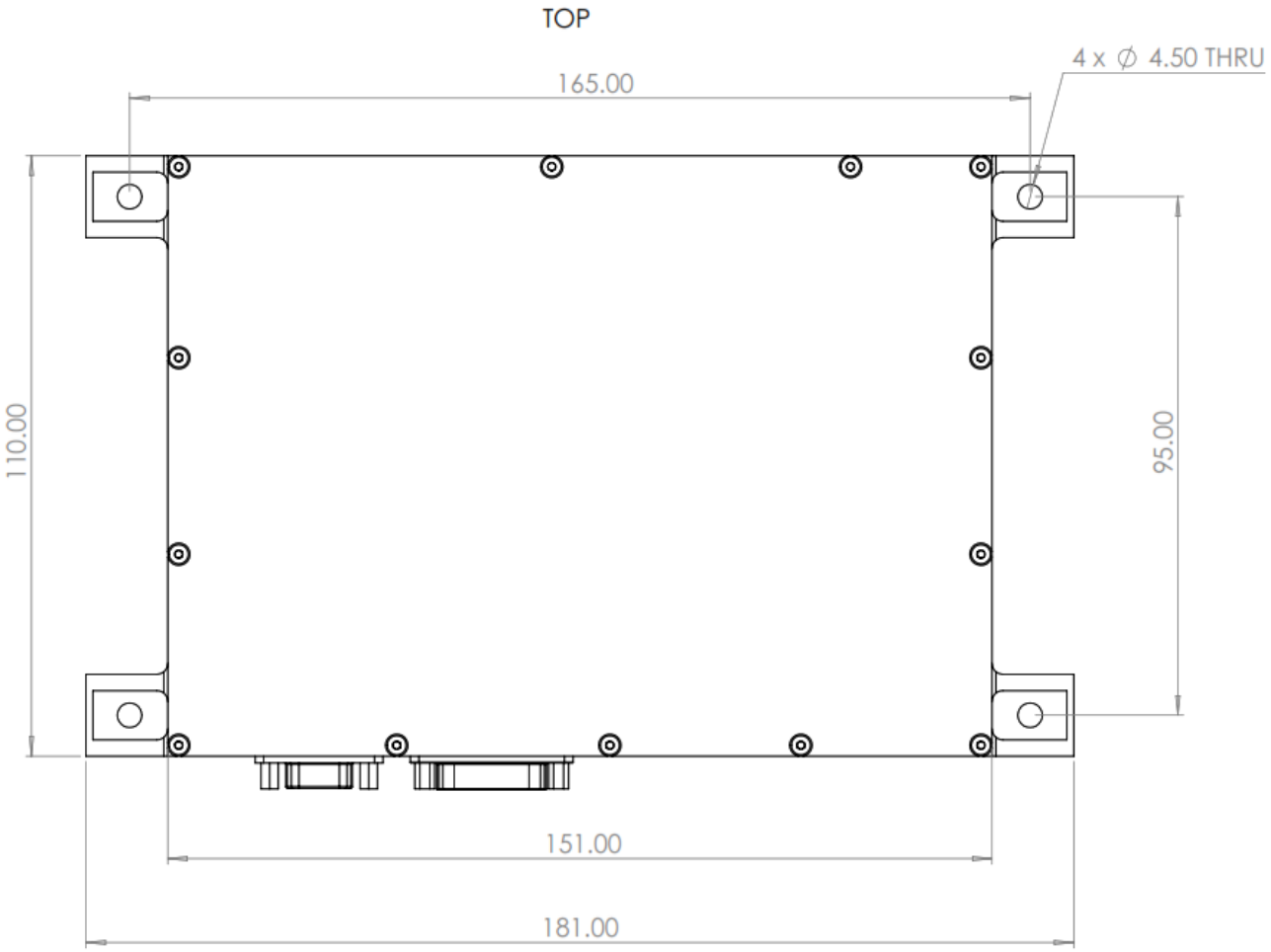

Figure 8: OBC-HYPER-POLAR Drawing Top View

The OBC HYPER-POLAR enclosure measures 110 mm × 151 mm (primary body), with mounting-point extensions bringing the total footprint to 110 mm × 181 mm. Four clearance holes accept M5 metric fasteners (or 8-32 UNC). The hole pattern is 95 mm × 165 mm with 4.50 mm through bore.

NOTE Recommended minimum thread engagement of 8 mm for M5 fasteners in aluminium. Refer to the spacecraft/rack structure ICD for the applicable torque specification.

CAUTION Do not apply excessive torque to the mounting fasteners. Over-torquing may deform the aluminium standoff bosses.

2.6.1 Enclosure Side Views — Front and Back Panels

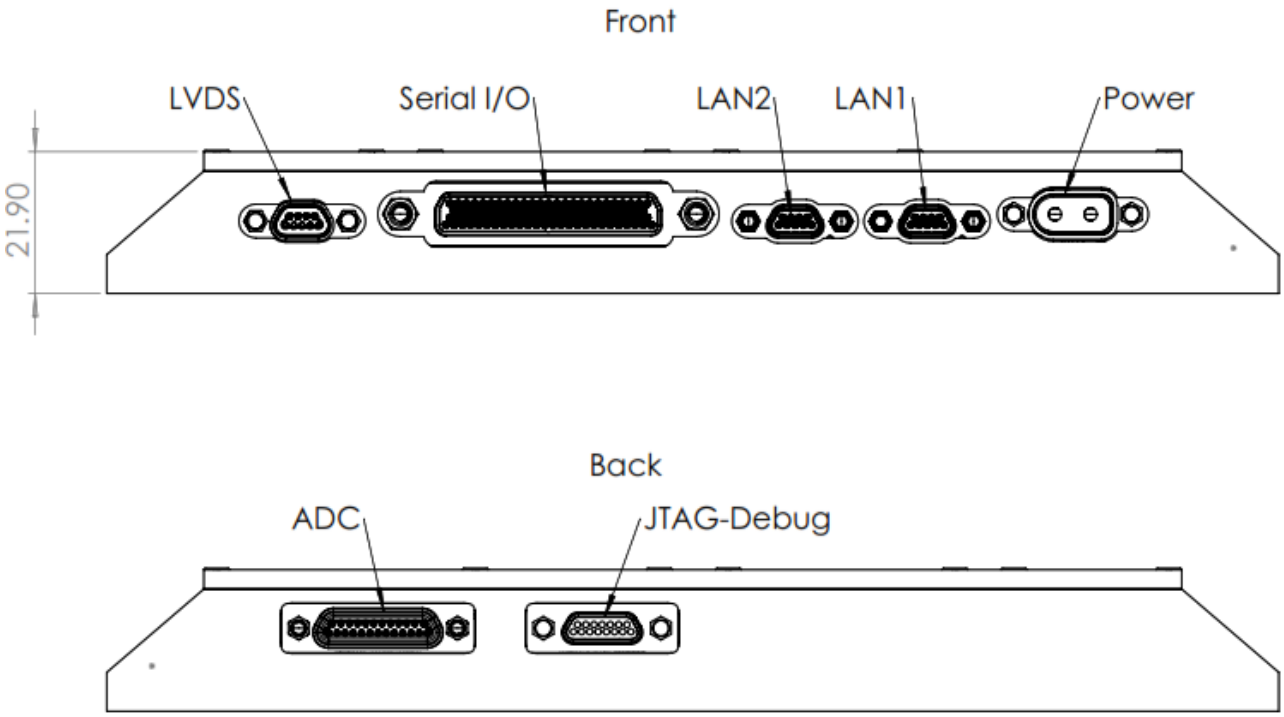

Figure 9: OBC-HYPER-POLAR Drawing Front & Back View

The front-panel face (the 110 mm edge) carries from left to right:

1. LVDS / SpaceWire — 9-pin Micro-D.
2. Serial I/O — 100-pin Micro-D.
3. LAN2 — 9-pin Micro-D.
4. LAN1 — 9-pin Micro-D.
5. Power — Glenair GMPM2 (2-pin).

The back-panel face carries from left to right:

1. ADC — 25-pin Micro-D.
2. JTAG / USB / Debug — 15-pin Micro-D.

2.7 Mass Properties

Item	Mass (g)
Enclosure (aluminium, without PCB)	450
Main OBC	210
Total system mass	660

Table 5 — Mass properties

2.8 Connector Summary

Table 6 lists every external connector on the OBC HYPER-POLAR in a single inventory. Section references take the reader to the per-interface pin-out and electrical characteristics tables. Cable colour codes (CAVU recommended) are given at the per-connector pin-out tables in Chapter 3.

Ref	Designation	Panel	Connector (OBC side)	Mating	Pins	Section
J1	LVDS / SpaceWire	Front	M835123/12-H01CP	M835123/04-H03N	9	§3.4
J2	Serial I/O	Front	100-pin Micro-D	100-pin Micro-D mate	100	§3.3
J3	LAN2	Front	MDM-9PCBRP	MDM-9SH003K	9	§3.2
J4	LAN1	Front	MDM-9PCBRP	MDM-9SH003K	9	§3.2
J5	Power	Front	GMPM2-B112R-CBRT-SU	GMPM2-B112P + GMPMBT2-B-EM backshell	2	§3.1
J6	JTAG / USB / Debug	Back	MDM-15PH003B	MDM-15SH003K + MDM-BT-15TE-SJS	15	§3.6
J7	ADC	Back	MDM-25PH003K	MDM-25SH003M7	25	§3.5

Table 6 — External connector inventory

3. Electrical Interfaces and Power

3.1 Power Supply

3.1.1 Input Voltage Range

The OBC HYPER-POLAR accepts a wide-range unregulated DC input at the GMPM2 connector. The factory-default operating range is 22 V to 32 V DC, centred on a 28 V nominal bus. Other input ranges (e.g. 12 V or 5 V bus) are available on request and are configured at the factory by hardware selection of the LCL thresholds.

Parameter	Default	Notes
Operating voltage range	22 V to 32 V DC	Factory-default; 28 V nominal bus
UVLO turn-on threshold	~22 V (rising)	Hardware-set on LCL stage
UVLO turn-off threshold	~21 V (falling)	Hysteresis built-in
OVP threshold	~32 V	Hardware-set on LCL stage
Soft-start ramp	5 ms typical, 10 ms max	From UVLO turn-on to full regulation
Reverse polarity	Protected	LCL contains active reverse-polarity isolation
Inrush current peak	< 0.5 A (28 V cold start)	Duration < 1 ms; LCL ramps softly

Table 7 — Power input — default factory parameters

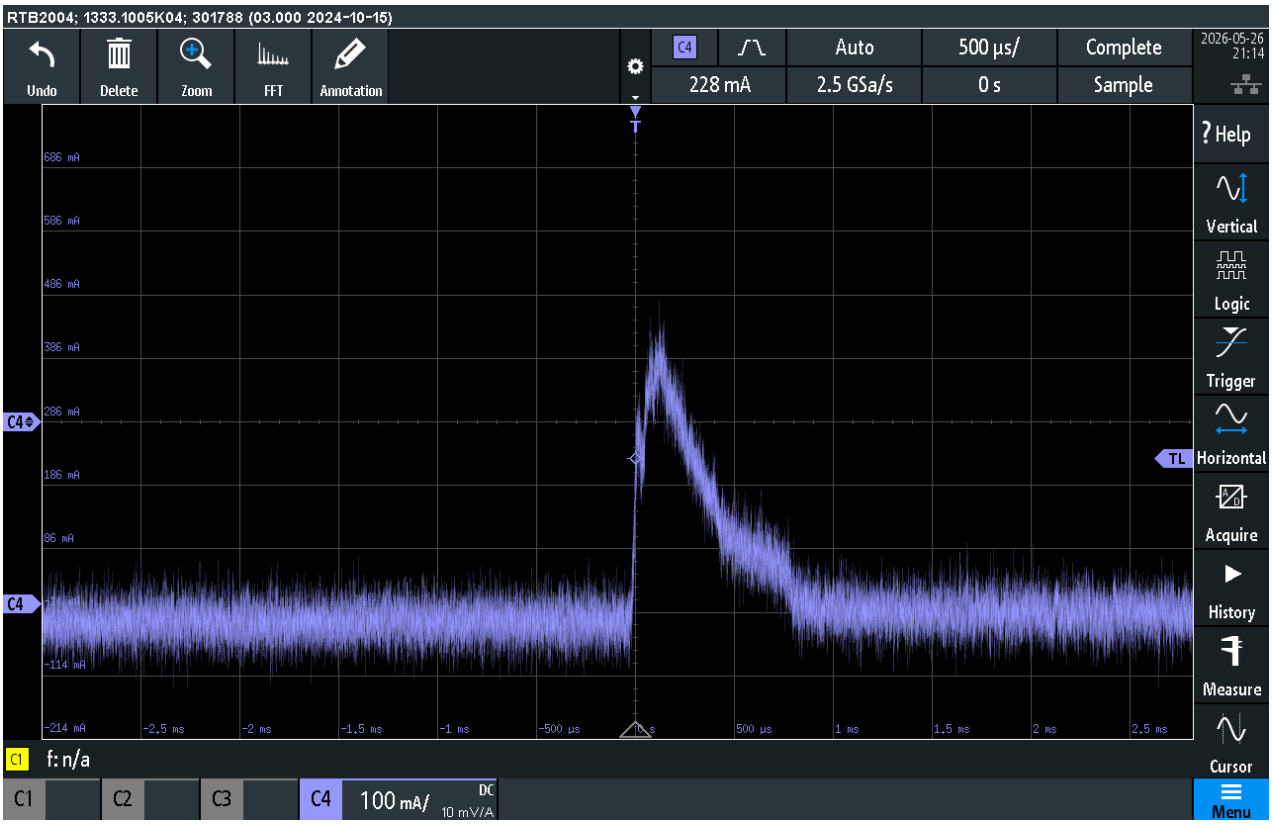

Figure 10: OBC-HYPER-POLAR Inrush Current at 28 V Input

WARNING Do not apply input voltages outside the configured factory range. Sustained over-voltage above the OVP threshold will latch the LCL off and may require a power cycle to recover. Sustained over-voltage above the absolute maximum may permanently damage the unit.

WARNING Verify harness polarity before first power-on. The GMPM2 connector is polarised but mis-wired harnesses are possible.

3.1.2 LCL Power Architecture

The first active element after the GMPM2 input connector is the Latch-up Current Limiter (LCL). The LCL combines five protection functions into a single coordinated block:

- Reverse-polarity isolation (active FET).
- In-rush current limiting with controlled soft-start ramp.
- Over-current limiting with foldback and automatic retry on transient events.
- Over-voltage protection (OVP) — hard latch-off above threshold, hardware-set at factory.
- Under-voltage lock-out (UVLO) — hard inhibit below threshold with hysteresis, hardware-set at factory.

The LCL behaviour is intentionally autonomous: it operates without software intervention and recovers transient anomalies on its own (e.g. brief over-current trips trigger a controlled retry). Sustained out-of-range conditions latch the LCL off — manual power cycle is required after the upstream fault is cleared.

Downstream of the LCL, the regulated rails for the SoC, memory, PHYs and other peripherals are produced by on-board converters. This section is internal to the unit and is not user-configurable; the regulator topology is therefore not described in this manual.

3.1.3 Power Connector Pinout

Pin	Signal	Cable colour	Description
1	VCC_IN	■ Red	22–32 V DC input (default; 28 V nominal)
2	GND_IN	■ Black	Power return (ground)

Table 8 — Power connector pinout (GMPM2-B112R-CBRT-SU)

NOTE Recommended wire gauge: AWG 16~20.

Figure 11: VCC and GND Pins Location

3.1.4 Power Connector — Mating Hardware

Item	Part Number
OBC side (receptacle)	Glenair GMPM2-B112R-CBRT-SU
Mating plug	Glenair GMPM2-B112P
Mating backshell (strain relief)	Glenair GMPMBT2-B-EM

3.1.5 Power Consumption

The OBC HYPER-POLAR input power consumption depends on FPGA fabric utilisation, the number of active PHYs, DDR4 activity and software workload. The figures below are representative; a precise budget for any specific configuration can be generated using the on-line CAVU power estimator.

Operating condition	Typical (W)	Notes
Idle / boot (MSS only, fabric idle)	~3	HSS resident; fabric in user reset; PHYs in low-power state
Nominal operation (Linux, two PHYs active)	~5	Steady-state telemetry / command traffic
Heavy workload (all PHYs, fabric switching)	~6	Sustained data flow on all Ethernet ports and PHYs
Peak (all interfaces simultaneously active)	≤ 8	Short transient peak; do not size cooling to this number

Table 9 — Indicative input power consumption

On-line power estimator: https://hyper-est.cavuaerospace.uk/

The estimator accepts a configuration template (FPGA variant, active PHYs, expected workload profile) and returns the predicted average and peak input power. Use it to size the spacecraft power harness and the upstream regulator capability.

3.2 Ethernet Interfaces (LAN1, LAN2)

OBC HYPER-POLAR provides two Gigabit Ethernet ports:

- **LAN1, LAN2 (main board, front panel).** Transformer-less, capacitive-coupled 1000BASE-T. Connected to the PolarFire SoC hard Ethernet MACs via SGMII PHYs.

Both Ethernet ports use 9-pin Micro-D connectors and the same pin-out (Table 10). Both ports expose standard Linux network interfaces, with one Linux network interface per port.

Pin	Signal	Cable colour	Description
1	D_P	Black	1000BASE-T pair D — positive
2	C_P	Brown	1000BASE-T pair C — positive
3	B_N	Red	1000BASE-T pair B — negative
4	B_P	Orange	1000BASE-T pair B — positive
5	A_P	Yellow	1000BASE-T pair A — positive
6	D_N	Green	1000BASE-T pair D — negative
7	C_N	Blue	1000BASE-T pair C — negative
8	A_N	Violet	1000BASE-T pair A — negative
9	GND	Grey	Signal ground / shield reference

Table 10 — Ethernet connector pin-out (9-pin Micro-D)

NOTE Auto-MDIX is supported on every port; straight-through or crossover cable will both work.

3.2.1 Ethernet — Signal Interface Characteristics

Parameter	Value	Notes
Interface type	4-pair differential, full-duplex	IEEE 802.3ab 1000BASE-T
Line rate	1000 Mbps	Auto-negotiation supported
LAN1/2 coupling	Transformer-less, capacitive-coupled	Capacitor array + common-mode choke; no pulse transformer
MDI / MDI-X	Auto-MDIX	Straight-through or crossover cable accepted
Differential impedance	100 Ω	On PCB and at connector
ESD protection	System-level on all pins	Meets IEC 61000-4-2 practice
Connector	9-pin Micro-D (MDM-9PCBRP)	See Table 10

Table 11 — Ethernet signal interface characteristics

3.3 Serial I/O Interface (100-pin Micro-D)

The Serial I/O connector is the main system I/O interface, aggregating every serial bus, GPIO and I²C onto a single high-density Micro-D on the front panel. It carries:

- 4× RS-422 full-duplex channels (16 signals: A1–A4, B1–B4, Y1–Y4, Z1–Z4 — A=TX+, B=TX−, Y=RX+, Z=RX−).
- 4× RS-232 channels (8 signals: TX1–TX4, RX1–RX4).
- 4× CAN channels (8 signals: CAN_H1–H4, CAN_L1–L4).
- 4× RS-485 channels (8 signals: RS485_A1–A4, RS485_B1–B4).
- 32× buffered GPIO in four banks of eight (GPIOB[1..32]).
- 8× Direct-IO (Direct-IO[1..8]).
- 1× I²C bus (SCL3.3 on pin 6, SDA3.3 on pin 31).
- Power return references (GND pins distributed across the connector).

> **NOTE** Pins corresponding to 52, 53, 54, 55, 76, 77, 78, 79 are No-Connect (NC). Do not wire them in the mating harness — they have no internal connection on the main board.

3.3.1 Serial I/O — Pin Assignment

Table 12 lists the full 100-pin Micro-D Serial I/O pin assignment. Pins marked "NC" are not connected on the OBC HYPER-POLAR main board.

Pin	Signal	Colour	Description	Pin	Signal	Colour	Description
1	Direct-IO8	■ Black	Direct I/O channel 8	51	RS422_B1	■ Black	RS-422 Ch1 TX− (B)
2	Direct-IO6	■ Brown	Direct I/O channel 6	52	NC	■ Brown	No Connect — do not wire
3	GND	■ Red	Signal ground	53	NC	■ Red	No Connect — do not wire
4	Direct-IO3	■ Orange	Direct I/O channel 3	54	NC	■ Orange	No Connect — do not wire
5	Direct-IO1	■ Yellow	Direct I/O channel 1	55	NC	■ Yellow	No Connect — do not wire
6	SCL3.3	■ Green	I²C clock, 3.3 V	56	GND	■ Green	Signal ground
7	RS232_RX3	■ Blue	RS-232 Ch3 receive	57	RS232_TX4	■ Blue	RS-232 Ch4 transmit
8	RS232_RX1	■ Violet	RS-232 Ch1 receive	58	RS232_TX2	■ Violet	RS-232 Ch2 transmit
9	GND	■ Grey	Signal ground	59	CAN_L4	■ Grey	CAN Ch4 Low
10	CAN_H3	☐ White	CAN Ch3 High	60	CAN_L2	☐ White	CAN Ch2 Low

11	CAN_H1	■ Black	CAN Ch1 High	61	RS485_A4	■ Black	RS-485 Ch4 A (non-inverting)
12	RS485_B3	■ Brown	RS-485 Ch3 B (inverting)	62	RS485_A2	■ Brown	RS-485 Ch2 A (non-inverting)
13	RS485_B1	■ Red	RS-485 Ch1 B (inverting)	63	GND	■ Red	Signal ground
14	GPIOB30	■ Orange	Buffered GPIO ch 30	64	GPIOB31	■ Orange	Buffered GPIO ch 31
15	GPIOB26	■ Yellow	Buffered GPIO ch 26	65	GPIOB27	■ Yellow	Buffered GPIO ch 27
16	GPIOB22	■ Green	Buffered GPIO ch 22	66	GPIOB23	■ Green	Buffered GPIO ch 23
17	GPIOB18	■ Blue	Buffered GPIO ch 18	67	GPIOB19	■ Blue	Buffered GPIO ch 19
18	GPIOB14	■ Violet	Buffered GPIO ch 14	68	GPIOB15	■ Violet	Buffered GPIO ch 15
19	GPIOB10	■ Grey	Buffered GPIO ch 10	69	GPIOB11	■ Grey	Buffered GPIO ch 11
20	GPIOB6	□ White	Buffered GPIO ch 6	70	GPIOB7	□ White	Buffered GPIO ch 7
21	GPIOB2	■ Black	Buffered GPIO ch 2	71	GPIOB3	■ Black	Buffered GPIO ch 3
22	GND	■ Brown	Signal ground	72	RS422_Y4	■ Brown	RS-422 Ch4 RX+ (Y)
23	RS422_A4	■ Red	RS-422 Ch4 TX+ (A)	73	RS422_Y3	■ Red	RS-422 Ch3 RX+ (Y)
24	RS422_A3	■ Orange	RS-422 Ch3 TX+ (A)	74	RS422_Z2	■ Orange	RS-422 Ch2 RX– (Z)
25	RS422_A2	■ Yellow	RS-422 Ch2 TX+ (A)	75	RS422_Y1	■ Yellow	RS-422 Ch1 RX+ (Y)
26	RS422_A1	■ Green	RS-422 Ch1 TX+ (A)	76	NC	■ Green	No Connect — do not wire
27	Direct-IO7	■ Blue	Direct I/O channel 7	77	NC	■ Blue	No Connect — do not wire
28	Direct-IO5	■ Violet	Direct I/O channel 5	78	NC	■ Violet	No Connect — do not wire
29	Direct-IO4	■ Grey	Direct I/O channel 4	79	NC	■ Grey	No Connect — do not wire
30	Direct-IO2	□ White	Direct I/O channel 2	80	GND	□ White	Signal ground
31	SDA3.3	■ Black	I^2C data, 3.3 V	81	RS232_RX4	■ Black	RS-232 Ch4 receive
32	GND	■ Brown	Signal ground	82	RS232_RX2	■ Brown	RS-232 Ch2 receive
33	RS232_TX3	■ Red	RS-232 Ch3 transmit	83	GND	■ Red	Signal ground
34	RS232_TX1	■ Orange	RS-232 Ch1 transmit	84	CAN_H4	■ Orange	CAN Ch4 High

35	CAN_L3	Yellow	CAN Ch3 Low	85	CAN_H2	Yellow	CAN Ch2 High
36	CAN_L1	Green	CAN Ch1 Low	86	RS485_B4	Green	RS-485 Ch4 B (inverting)
37	RS485_A3	Blue	RS-485 Ch3 A (non-inverting)	87	RS485_B2	Blue	RS-485 Ch2 B (inverting)
38	RS485_A1	Violet	RS-485 Ch1 A (non-inverting)	88	GPIOB32	Violet	Buffered GPIO ch 32
39	GND	Grey	Signal ground	89	GPIOB28	Grey	Buffered GPIO ch 28
40	GPIOB29	☐ White	Buffered GPIO ch 29	90	GPIOB24	☐ White	Buffered GPIO ch 24
41	GPIOB25	Black	Buffered GPIO ch 25	91	GPIOB20	Black	Buffered GPIO ch 20
42	GPIOB21	Brown	Buffered GPIO ch 21	92	GPIOB16	Brown	Buffered GPIO ch 16
43	GPIOB17	Red	Buffered GPIO ch 17	93	GPIOB12	Red	Buffered GPIO ch 12
44	GPIOB13	Orange	Buffered GPIO ch 13	94	GPIOB8	Orange	Buffered GPIO ch 8
45	GPIOB9	Yellow	Buffered GPIO ch 9	95	GPIOB4	Yellow	Buffered GPIO ch 4
46	GPIOB5	Green	Buffered GPIO ch 5	96	GND	Green	Signal ground
47	GPIOB1	Blue	Buffered GPIO ch 1	97	RS422_Z4	Blue	RS-422 Ch4 RX– (Z)
48	RS422_B4	Violet	RS-422 Ch4 TX– (B)	98	RS422_Z3	Violet	RS-422 Ch3 RX– (Z)
49	RS422_B3	Grey	RS-422 Ch3 TX– (B)	99	RS422_Y2	Grey	RS-422 Ch2 RX+ (Y)
50	RS422_B2	☐ White	RS-422 Ch2 TX– (B)	100	RS422_Z1	☐ White	RS-422 Ch1 RX– (Z)

Table 12 — Serial I/O connector pin-out (100-pin Micro-D)

WARNING Observe ESD precautions when handling and mating the 100-pin Micro-D Serial I/O connector. Use the prescribed Micro-D mating connector.

3.3.2 RS-422 — Electrical Characteristics

Parameter	Value	Notes
Interface type	Differential, full-duplex (TX±, RX±)	Per TIA/EIA-422
Naming	A = TX+, B = TX−, Y = RX+, Z = RX−	CAVU convention
Data rate	1.2 kbps to 16 Mbps	Default 115 200 bps; configurable in software
Word format	8-N-1 (default)	Software-configurable
Driver differential output	≥ 2.0 V (into 100 Ω load)	TIA/EIA-422
Receiver input sensitivity	≥ ±200 mV worst-case	Per TIA/EIA-422; typical sensitivity is significantly better than the standard floor
Receiver input impedance	≥ 12 kΩ per line	
Common-mode range (receiver)	−7 V to +7 V	Relative to signal ground
Fail-safe bias	Internal (idle = logic high)	
Termination	100 Ω selectable	Factory default: enabled on receiver
ESD protection	System-level on all pins	
Connector	100-pin Micro-D (J2)	See Table 12

Table 13 — RS-422 (×4) signal interface characteristics

3.3.3 RS-232 — Electrical Characteristics

Parameter	Value	Notes
Interface type	Single-ended, full-duplex (TXD, RXD)	Per EIA/TIA-232
Naming	RS232_TX1..TX4 (transmit), RS232_RX1..RX4 (receive)	OBC perspective
Data rate	Up to 921.6 kbps	Standard baud rates
Word format	8-N-1 (default)	Software-configurable
Driver output (no load)	±5 V to ±9 V	EIA-232 compliant
Receiver input threshold	±3 V minimum	Receiver logic switching threshold
Flow control	Not routed externally	Use software (XON/XOFF) if required
ESD protection	System-level on all pins	
Connector	100-pin Micro-D (J2)	See Table 12

Table 14 — RS-232 (×4) signal interface characteristics

3.3.4 CAN 2.0B — Electrical Characteristics

Parameter	Value	Notes
Interface type	Differential, half-duplex (CAN_H, CAN_L)	ISO 11898-2 high-speed CAN
Data rate	Up to 1 Mbps (Classical CAN 2.0B)	CAN FD possible on fabric-implemented channels
Recessive bus level	~2.5 V on both CAN_H and CAN_L	Differential = 0 V
Dominant differential	~1.5 V to 2.0 V (CAN_H − CAN_L)	Dominant state
Termination	120 Ω at each physical bus end	External — not on-board at the connector
Common-mode range	−2 V to +7 V	Per ISO 11898-2
Controller source	Ch1/Ch2 = MSS hard CAN controllers; Ch3/Ch4 = FPGA fabric	
ESD protection	System-level on all pins	
Connector	100-pin Micro-D (J2)	See Table 12

Table 15 — CAN 2.0B (×4) signal interface characteristics

CAUTION When the OBC is connected to a CAN network that already includes nodes with on-board termination, verify that the bus total termination is between 100 Ω and 120 Ω. Incorrect termination degrades signal integrity at higher bus speeds.

3.3.5 RS-485 — Electrical Characteristics

Parameter	Value	Notes
Interface type	Differential (A/B), half-duplex or full-duplex	TIA/EIA-485
Naming	A = non-inverting, B = inverting	
Data rate	Up to 16 Mbps	Application-dependent
Word format	8-N-1 (default)	Software-configurable
Receiver input sensitivity	≥ ±200 mV worst-case (TIA/EIA-485 floor)	Transceiver typical V_IT is in the ±70 mV to ±200 mV range; absolute minimum +200 / −200 mV is the standard floor that must be reliably detected.
Common-mode range (receiver)	−7 V to +12 V	Per TIA/EIA-485
Bus load	Up to 32 unit loads per segment	OBC counts as 1 unit load per channel
Termination	100 Ω at each physical bus end	External; not on-board at connector
ESD protection	System-level on all pins	
Connector	100-pin Micro-D (J2)	See Table 12

Table 16 — RS-485 (×4) signal interface characteristics

NOTE The "± 200 mV" figure is the TIA/EIA-485 worst-case receiver-sensitivity requirement. The transceivers used on the OBC HYPER-POLAR typically detect signals significantly smaller than this; the standard floor is reported because it is the value the spacecraft harness designer must size the differential signal against.

3.3.6 GPIO Interface

Buffered GPIO (GPIOB[1..32])

Thirty-two general-purpose I/O lines are buffered through external buffer ICs and organised in four banks of eight signals each. The direction of each bank (all-input or all-output) is set independently of the other banks; direction is not configurable on a per-signal basis within a bank.

Bank	Signals	Direction control	Output voltage
Bank A	GPIOB[1..8]	Per-bank — all input or all output	Factory-selectable: 3.3 V or 5.0 V
Bank B	GPIOB[9..16]	Per-bank — all input or all output	
Bank C	GPIOB[17..24]	Per-bank — all input or all output	Factory-selectable: 3.3 V or 5.0 V
Bank D	GPIOB[25..32]	Per-bank — all input or all output	

Table 17 — Buffered GPIO bank organisation

At power-on reset the buffer output enables are held inactive and each bank defaults to input (high-impedance). The direction selection is applied by the FPGA bitstream and the application software during initialization.

Direct-IO (Direct-IO [1..8])

Eight signals are connected directly to PolarFire SoC fabric I/O pins (no external buffer). Logic level is 3.3 V. Each pin can be configured as GPIO or as any alternate function supported by the fabric I/O (UART, SPI, I^2C, PWM …) by the FPGA design.

WARNING Direct-IO lines are not protected at the connector level beyond the PolarFire device internal ESD structures. Do not apply voltages outside the FPGA I/O supply range (3.3V) to Direct-IO pins. Handle with ESD precautions.

I^2C (SCL3.3, SDA3.3)

A dedicated I^2C bus is provided on pin 6 (SCL3.3) and pin 31 (SDA3.3) of the 100-pin connector. 3.3 V logic level with internal pull-up resistors; standard mode (100 kHz) and fast mode (400 kHz) supported.

CAUTION Do not drive any GPIO or Direct-IO pin with external voltage above the configured 3.3V or below GND. Add series resistance (33–100 Ω) on lines that may be subject to over-voltage transients.

3.4 LVDS / SpaceWire Interface (9-pin Micro-D)

The OBC HYPER-POLAR provides two LVDS transmit/receive pairs on the front-panel 9-pin Micro-D LVDS/SpaceWire connector. Signal levels, differential impedance and connector pin-out are compatible with ECSS-E-ST-50-12C SpaceWire. SpaceWire link encoding and protocol are implemented in the FPGA fabric.

Pin	Signal (CAVU)	Cable colour	SpaceWire / Description
1	LVDS_RX1_P	Black	SpW Din+ (Data In +) — link 1 RX positive
2	LVDS_RX2_P	Brown	SpW Sin+ (Strobe In +) — link 2 RX positive
3	GND	Red	Signal ground
4	LVDS_TX1_N	Orange	SpW Dout− (Data Out −) — link 1 TX negative
5	LVDS_TX2_N	Yellow	SpW Sout− (Strobe Out −) — link 2 TX negative
6	LVDS_RX1_N	Green	SpW Din− (Data In −) — link 1 RX negative
7	LVDS_RX2_N	Blue	SpW Sin− (Strobe In −) — link 2 RX negative
8	LVDS_TX1_P	Violet	SpW Dout+ (Data Out +) — link 1 TX positive
9	LVDS_TX2_P	Grey	SpW Sout+ (Strobe Out +) — link 2 TX positive

Table 18 — LVDS/SpaceWire connector pin-out

3.4.1 LVDS / SpaceWire — Electrical Characteristics

Parameter	Value	Notes
Differential voltage swing	350 mV typical (250–450 mV)	ANSI/TIA-644 LVDS
Common-mode voltage	~1.2 V	
Differential impedance	100 Ω	PCB and harness
Link rate	2–200 Mbps per link	Per ECSS-E-ST-50-12C; actual rate determined by fabric implementation
ESD protection	System-level on all pins	
Connector	9-pin Micro-D M835123/12-H01CP (J1)	See Table 18

Table 19 — LVDS / SpaceWire signal interface characteristics

CAUTION Do not connect TX-to-TX between two OBC HYPER-POLAR units. Connect TX from one unit to RX on the other. Incorrect polarity will not damage the LVDS circuits (current-limited drivers, high-impedance receivers) but will prevent link establishment.

3.5 ADC Interface (25-pin Micro-D)

The OBC HYPER-POLAR integrates a 16-channel, 16-bit simultaneous-sampling AD7616 ADC. All 16 input channels and the 3.3 V / 5 V reference outputs are routed via an internal shielded ribbon cable from the PCB to the back-panel 25-pin Micro-D ADC connector. The internal cable is assembled and tested at the factory; no user access to the PCB header is required.

Key spec.: 16 channels in two banks of 8 (A0..A7, B0..B7); 16-bit resolution; true simultaneous sampling across all channels; up to 1 MSPS per channel-pair; input range ±5 V or ±10 V factory-selectable (default ±10 V); input over-voltage protection ±20 V absolute maximum; interfaced to FPGA fabric over SPI.

Pin	Signal	Cable colour	Description
1	ADC2	Black	ADC input channel 2
2	ADC4	Brown	ADC input channel 4
3	ADC6	Red	ADC input channel 6
4	ADC8	Orange	ADC input channel 8
5	ADC10	Yellow	ADC input channel 10
6	ADC12	Green	ADC input channel 12
7	ADC14	Blue	ADC input channel 14
8	ADC16	Violet	ADC input channel 16
9	3.3V_OUT	Grey	3.3 V reference output (low current)
10	GND	White	Digital ground
11	AGND	White / Black	Analogue ground
12	AGND	White / Brown	Analogue ground
13	AGND	White / Red	Analogue ground
14	AGND	White / Orange	Analogue ground
15	ADC1	White / Yellow	ADC input channel 1
16	ADC3	White / Green	ADC input channel 3
17	ADC5	White / Blue	ADC input channel 5
18	ADC7	White / Violet	ADC input channel 7
19	ADC9	White / Grey	ADC input channel 9
20	ADC11	White / Black / Brown	ADC input channel 11
21	ADC13	White / Black / Red	ADC input channel 13
22	ADC15	White / Black / Orange	ADC input channel 15
23	5V_OUT	White / Black / Yellow	5 V reference output (low current)
24	AGND	White / Black / Green	Analogue ground
25	AGND	White / Black / Blue	Analogue ground

Table 20 — ADC connector pin-out (25-pin Micro-D)

3.5.1 ADC — Electrical Characteristics

Parameter	Value	Notes
Resolution	16 bit	
Channels	16, dual simultaneous (8+8)	AD7616
Sample rate	Up to 1 MSPS per channel-pair	
Input range	±5 V or ±10 V	Factory-selectable; default ±10 V
Absolute max input	±20 V	Per AD7616 datasheet
Oversampling	2× to 128×	Internal AD7616 OS
Interface	SPI to FPGA fabric	Master = fabric
Reference outputs	3.3 V (pin 9) and 5 V (pin 23)	Low-current; for sensor reference only
Connector	25-pin Micro-D MDM-25PH003K (J7)	See Table 20

Table 21 — ADC signal interface characteristics

NOTE AGND is star-connected to system GND inside the enclosure. Do not use the chassis or power return as the ADC signal reference — that will degrade ADC linearity and effective noise-free resolution.

CAUTION Apply voltages outside ±20 V absolute maximum to any ADC input may permanently damage the AD7616. Customer signal conditioning must limit voltages presented at the ADC connector to within the configured range with adequate margin.

3.6 JTAG / USB / Debug Interface (15-pin Micro-D)

The back-panel 15-pin Micro-D JTAG/USB/Debug connector aggregates three signal groups: JTAG signals for FlashPro5/6 programming; the dual UART debug console (via CP2105 USB-to-UART bridge); and the PolarFire SoC native USB 2.0. All three groups are broken out by the supplied CAVU-HYPER-POLAR-DBG debug adapter card (§3.7).

Pin	Signal	Cable colour	Description
1	5V_USB	Black	USB VBUS for PolarFire SoC native USB 2.0
2	USB_N	Brown	USB D− for PolarFire SoC native USB 2.0
3	5V_USB_UART	Red	USB VBUS for CP2105 USB-to-UART bridge
4	USB_UART_N	Orange	USB D− for CP2105 USB-to-UART bridge
5	VJTAG	Yellow	JTAG voltage reference (3.3 V, 50 mA max)
6	TMS	Green	JTAG test mode select
7	TDO	Blue	JTAG test data output (from PolarFire)
8	TCK	Violet	JTAG test clock
9	USB_ID	Grey	USB ID (PolarFire SoC USB OTG identification)
10	USB_P	White	USB D+ for PolarFire SoC native USB 2.0
11	GND	Black (Repeat)	Signal ground
12	USB_UART_P	Brown (Repeat)	USB D+ for CP2105 USB-to-UART bridge
13	ResetN	Red	System reset input, active-low (open-drain with pull-up)
14	TRST	Orange	JTAG test reset, active-low
15	TDI	Yellow	JTAG test data input (to PolarFire)

Table 22 — JTAG/USB/Debug connector pin-out (15-pin Micro-D)

NOTE VJTAG (pin 5) is a low-current reference output (≤ 50 mA). It is intended for external programmer logic reference only — do not use it as an external power source.

CAUTION Do not mate or un-mate the JTAG/USB/Debug connector while a JTAG programming operation is in progress. Interrupting the JTAG interface during Flash write may leave the device in an indeterminate state.

3.7 CAVU-HYPER-POLAR-DBG Debug Adapter Card

The CAVU-HYPER-POLAR-DBG is a small breakout card supplied with each OBC HYPER-POLAR unit. It attaches to the 15-pin JTAG/USB/Debug connector on the back panel and provides discrete connectors for development and test use.

Figure 12: OBC-HYPER-POLAR Debug Interface Board

Connector on adapter	Purpose	Mates with
J3 — 15-pin Sub-D plug	Attaches to OBC back panel	MDM-15PH003B on OBC
J4 — 10-pin 2×5 header (2.54 mm)	FlashPro5/6 JTAG programming interface	Microchip FlashPro5 or FlashPro6 cable
J2 — USB Type-B receptacle	USB-to-UART dual debug console (CP2105 bridge)	Host PC USB-A to USB-B cable
J1 — USB Mini-B receptacle	PolarFire SoC native USB 2.0	Host PC USB-A to Mini-B cable

Table 23 — CAVU-HYPER-POLAR-DBG connectors

3.7.1 FlashPro5/6 Header Pin-out (J2)

The 10-pin 2×5 header on the adapter follows the standard Microchip FlashPro pinout. The same pinout is used on Microchip evaluation kits and is directly compatible with FlashPro5 and FlashPro6 cables.

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TDO	4	PROG_MODE — NC
5	TMS	6	VJTAG (3.3 V)
7	VPUMP — NC	8	TRSTB
9	TDI	10	GND

Table 24 — FlashPro5/6 header pin-out (J2 on CAVU-HYPER-POLAR-DBG)

3.7.2 Debug Console (CP2105)

The USB Type-B receptacle bridges the host PC to two independent UART channels via the on-board CP2105 USB-to-UART bridge. With the CP2105 USB VCP driver installed, the host enumerates two serial-port devices:

- **Port 1 (Channel A):** HSS debug console.
- **Port 2 (Channel B):** Linux / application console.
  Default UART settings: 115 200 bps, 8-N-1, no flow control.

3.7.3 PolarFire USB 2.0

The USB Mini-B receptacle exposes the PolarFire SoC native USB 2.0 interface. The device class is determined by the USB gadget driver loaded by the running software (USB CDC-ACM, mass storage, or any custom class).

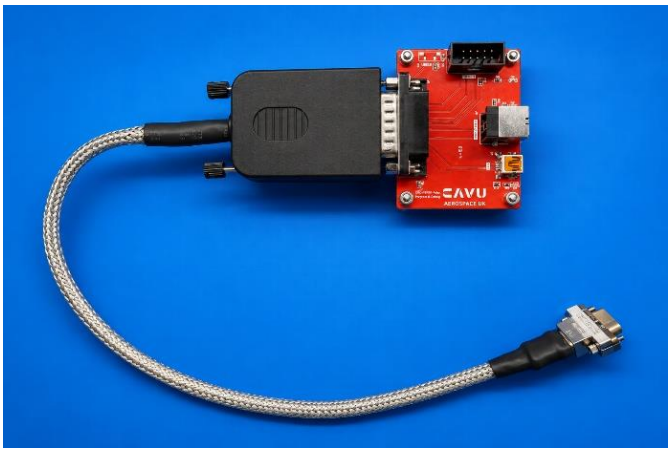

Figure 13: Debug Board with 15pin connector harness attached

4. Environmental and Mechanical Qualification

4.1 Environmental Specifications

Parameter	Operating range	Notes
Storage temperature	−55 °C to +125 °C	Non-operating
Operating temperature (MPFS250T, MPFS460T-I)	−40 °C to +85 °C	Industrial-grade screening
Operating temperature (MPFS460TS)	−55 °C to +125 °C	*Military-grade screening — stock-dependent*
Operating altitude	Vacuum to sea level	No de-rating
Operating relative humidity	0 % to 95 % non-condensing	
Cooling	Conduction through enclosure chassis	Enclosure base provides thermal interface
Total ionising dose (TID)	30Krad	-

Table 25 — Environmental specifications

4.2 Qualification — QM and FM Test Programme

Each Qualification Model (QM) and Flight Model (FM) of the OBC HYPER-POLAR is subjected to an environmental qualification programme tailored to ECSS-E-ST-10-03 (Testing) and ECSS-Q-ST-10C (Product Assurance) practices. The headline test envelope is summarized in Table 27.

Test	QM envelope	FM acceptance	Reference
Random vibration	14.1 g rms qualification; 3 axes; 2 min/axis	10.0 g rms acceptance; 3 axes; 1 min/axis	ECSS-E-ST-10-03
Sinusoidal vibration	Profile per spacecraft ICD; 3 axes; sweep 5–100 Hz	Same profile, reduced duration	ECSS-E-ST-10-03
Shock (SRS)	2 000 g over 100–10 000 Hz (3 axes, both polarities)	Not repeated at FM unless ICD requires	ECSS-E-ST-10-03
Thermal vacuum	8 cycles, +/− 55 °C, 1×10^{-5} mbar	4 cycles, mission temperature envelope	ECSS-E-ST-10-03
Thermal cycling (ambient)	8 cycles −40 to +85 °C (industrial) or −55 to +125 °C (military)	4 cycles	ECSS-Q-ST-70
EMC — conducted emissions	MIL-STD-461 CE102 or ECSS-E-ST-20-07 equivalent	Acceptance check	MIL-STD-461 / ECSS-E-ST-20-07
EMC — radiated emissions	MIL-STD-461 RE102 / ECSS-E-ST-20-07	Acceptance check	MIL-STD-461 / ECSS-E-ST-20-07
EMC — conducted susceptibility	CS101 / CS114 / CS115 / CS116	Acceptance subset	MIL-STD-461
EMC — radiated susceptibility	RS103 (1–18 GHz, 20 V/m)	Acceptance subset	MIL-STD-461
Functional verification	Pre/post each environment	Full functional sweep	CAVU acceptance plan

Table 26 — QM / FM environmental qualification matrix

NOTE The values above are the standard CAVU qualification envelope. Mission-specific qualification envelopes are agreed with the customer at PDR/CDR and are documented in the Qualification Test Plan (CAVU-HYPER-POLAR-OBC-QTP).

4.3 Mechanical Specifications

Parameter	Value
Overall envelope (with mounting tabs)	110 mm × 181 mm × 21.9 mm (W × L × H)
Primary body footprint	110 mm × 151 mm
Enclosure height	21.9 mm
Enclosure material	Aluminium alloy 7075-T6
Surface finish	Type II Alodine per MIL-A-8625
Mounting holes	4× clearance Ø 4.50 mm (8-32 UNC)
Mounting hole pattern	95 mm × 165 mm matrix
Recommended fastener	#8-32, A4 stainless, with washer
Recommended fastener torque	5.0 Nm (verify with structure ICD)
Total mass	660 gr
Thermal interface	Enclosure base — conduction to spacecraft baseplate

Table 27 — Mechanical specifications

5. System Setup and Getting Started

The OBC HYPER-POLAR ships with the HSS supervisor resident in eNVM and a default Linux image written to eMMC-A. The system is ready to use out of the box for standard Linux applications. This chapter describes initial power-on, the HSS supervisor and boot fallback chain, software image updates, bare-metal development, network configuration and the development-tool reference.

5.1 Initial Power-On

Prerequisites:

- CAVU-HYPER-POLAR-DBG debug adapter card (shipped with the unit).
- USB Type-A to Type-B cable for the CP2105 dual debug console.
- Host PC with the CP2105 USB VCP driver installed.
- A serial terminal application (PuTTY, Tera Term, minicom or equivalent).
- DC power supply in the configured input range (default 22–32 V).

Procedure:

1. Connect the power harness to the GMPM2 front-panel connector. Verify polarity (pin 1 = VCC_IN, pin 2 = GND_IN).
2. Connect the CAVU-HYPER-POLAR-DBG debug adapter to the back-panel 15-pin JTAG/USB/Debug Micro-D.
3. Connect a USB Type-B cable from J3 on the debug adapter to the host PC.
4. The host PC will detect two virtual serial ports under the CP2105 driver — Port 1 (HSS console, Channel A) and Port 2 (Linux console, Channel B).
5. Open the serial terminal application and connect both ports at 115 200 bps, 8-N-1, no flow control.
6. Apply power. The system boots automatically. HSS first prints the supervisor banner; OpenSBI and U-Boot output then appear; the Linux login prompt appears on the second port once the U54 cores are released and Linux is up.

> **NOTE** If no activity is observed on either terminal within 30 s of power-on, verify the USB VCP driver is installed and the correct COM ports are selected. The HSS banner is always the first output — its absence indicates a power, harness or hardware-fault condition.

5.2 HSS Supervisor — Boot Sequence and Image Selection

The HSS supervisor is the heart of the OBC HYPER-POLAR software model. It runs exclusively on the PolarFire SoC E51 monitor core, is resident in eNVM (the SoC die non-volatile memory), and is responsible for first-stage boot, payload verification, U54 release, and runtime supervisor services. The full reference is the supervisor reference document; the operational summary is below.

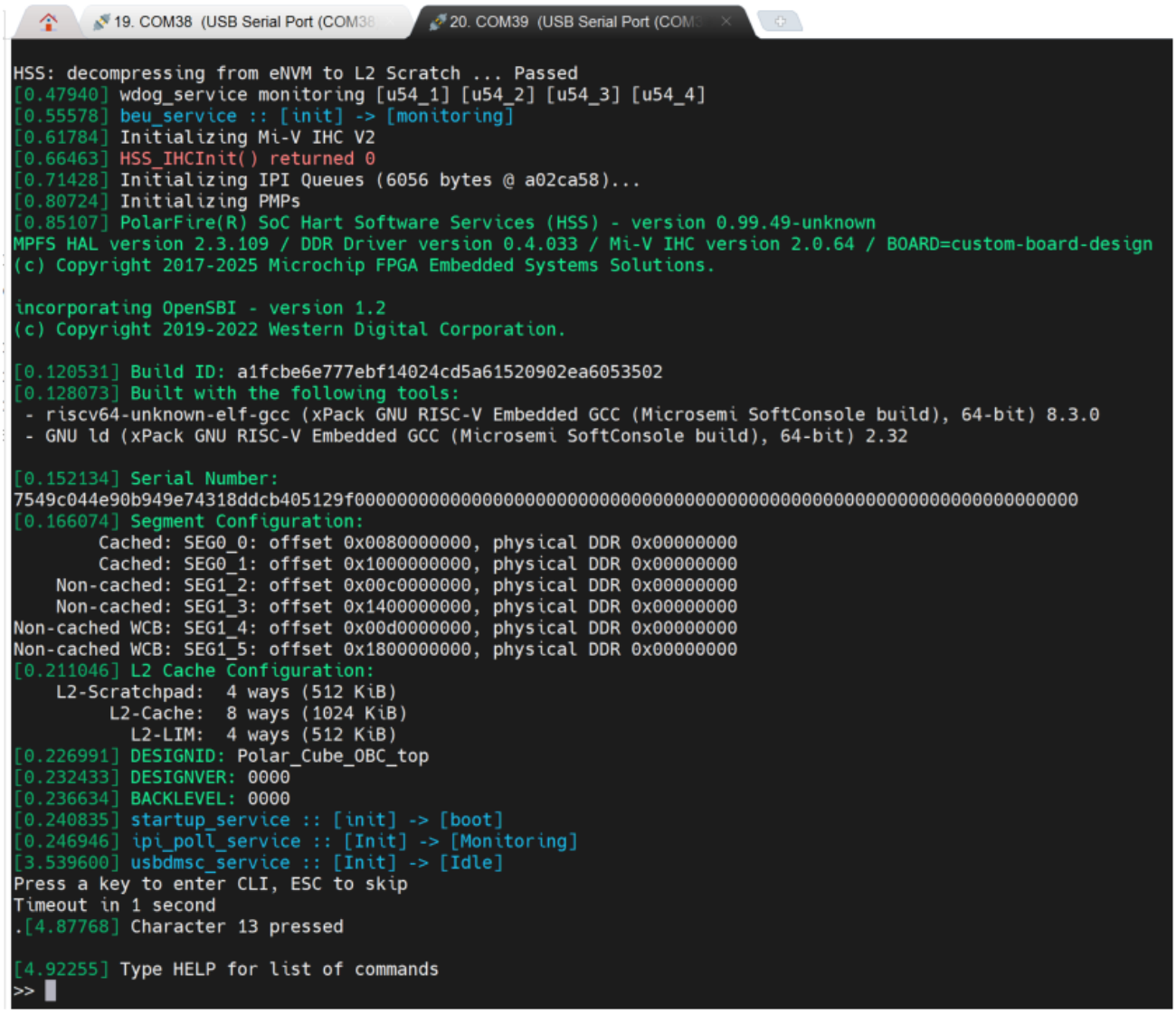

Figure 14: HSS Terminal Output

5.2.1 Boot Sequence (Detailed)

At every power-up the OBC HYPER-POLAR performs the following sequence:

1. PolarFire SoC System Controller releases the MSS from reset. The flash-based FPGA fabric is live and configured at this point — there is no external bitstream load step.
2. The E51 monitor core boots into HSS code resident in eNVM.
3. HSS initialises the DDR4 and LPDDR4 memory controllers and reads the active-bank pointer from SPI MRAM.
4. HSS walks the payload fallback chain (see §5.2.2) until a signed payload is verified.

5. HSS extracts the U54 payload, typically OpenSBI and U-Boot, into DDR4, configures each U54 core as required by the payload image, and releases the U54 cores from reset.
6. OpenSBI provides the M-mode supervisor-binary interface to the U54 cores; U-Boot loads the Linux kernel (or other application image) from eMMC, QSPI or MRAM as configured by the boot script.
7. Linux (or the chosen OS) initialises peripherals and reaches user-space.
8. HSS remains resident on the E51 throughout operation. It owns the hardware watchdog, runs the FDIR heartbeat protocol, provides boot-management and runtime monitor services, and exposes the HSS runtime console on the MMUART. OpenSBI provides the Supervisor Binary Interface used by the U54 software stack.

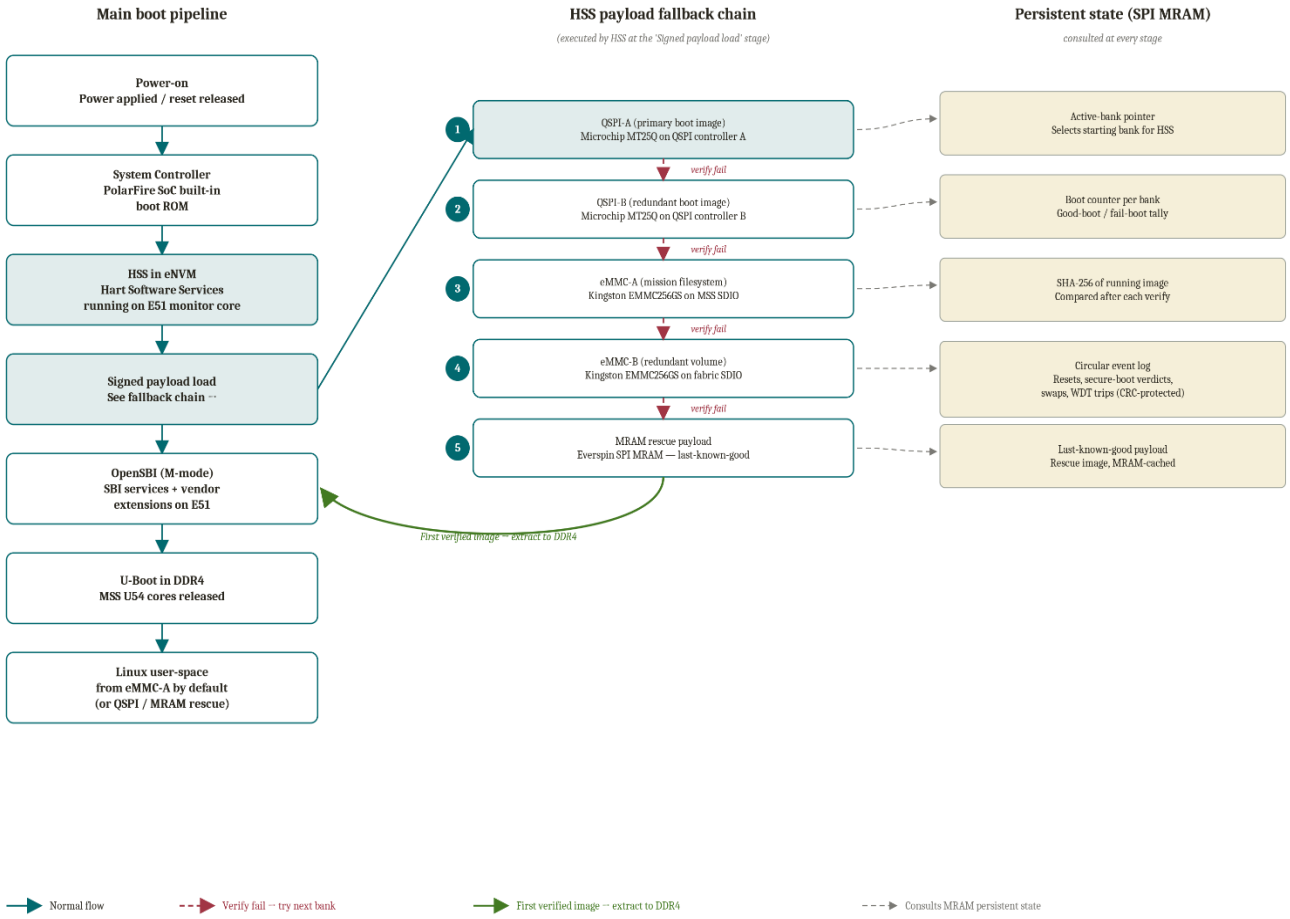

Figure 15: OBC-HYPER-POLAR Boot Sequence

5.2.2 Payload Fallback Chain

OBC HYPER-POLAR provides five redundant payload locations. HSS walks the fallback chain in the order below until a payload with a valid SHA-256 hash (and signature, if secure boot is enabled) is found:

1. QSPI-A — primary HSS payload.
2. QSPI-B — redundant HSS payload (golden image).
3. eMMC-A — eMMC primary payload partition.
4. eMMC-B — eMMC redundant payload partition.
5. SPI MRAM rescue payload — minimum-size recovery image that brings the system into a serviceable safe-mode state for ground recovery action.

When HSS finds a valid payload it boots from it, increments the bank's "good-boot" counter in MRAM, and clears the failure-count for that bank. When verification fails or the U54 cores fail to reach their heartbeat within the configured grace period, HSS swaps the active-bank pointer to the next location in the chain, resets, and continues. After two successive failures across the entire chain, HSS enters safe-mode and waits for ground recovery action while keeping the console alive.

5.2.3 Controlling the Boot Sequence and Image Selection

There are three independent control surfaces:

Compile-time (HSS YAML configuration). Build-time policy is defined in the project hss-config.yaml (or hss-payload.yaml). The YAML sets, per U54: entry address and execution mode (M-mode bare-metal, S-mode under Linux), preferred payload bank, secure-boot policy, payload region offset/size, and per-hart watchdog window. The same YAML drives the HSS Payload Generator that packages each .payload blob written to QSPI or eMMC.

Operational time (HSS console). At every reset HSS prints a countdown to auto-boot on the MMUART. Pressing any key during the countdown drops the system to the HSS command-line. Useful commands: boot (immediate boot per configured policy), payload (query current payload header, hash, and verification verdict), mmc / usbdmsc (expose eMMC as USB mass storage to the host PC), ymodem (receive a fresh payload over the UART and write it to a selected bank), qspi (direct QSPI erase/write), info (boot counters, last-fault reason, MRAM log).

Run time (SBI vendor calls). CAVU adds a small set of SBI vendor-extension calls under the 0x09xxxxxx vendor range that the application running on the U54 cores can issue: schedule next boot from a specified bank, mark current image bad, request safe-mode reboot. These calls are processed by HSS on the E51, persisted in MRAM, and survive a power cycle.

> **NOTE** A development/rescue path exists where HSS boots a payload uploaded over the MMUART (ymodem flow) without writing it to flash. This path is fused off in flight builds.

5.2.4 Diagnostics

Three independent channels provide diagnostics:

- **HSS console (MMUART).** Full boot log, secure-boot verdicts, payload metadata, boot counters, last-fault reason. Default 115 200 bps, 8-N-1. Available at every reset, including before any U54 is alive.
- **Housekeeping telemetry from the application.** Once Linux is up, the U54 monitor task exposes the same data over the spacecraft TM bus: BOOT_STATUS, active bank, hash digest of the running payload, ECC corrected/uncorrected counts, WDT-trip count per hart, MRAM wear counters.
- **Persistent log in MRAM.** Every reset reason, secure-boot verdict, bank swap, and WDT trip is appended to a circular log in SPI MRAM with a CRC. The log survives complete power loss and is downloadable on demand.

5.3 Updating the Linux Image

The CAVU-supplied Linux root filesystem lives on eMMC-A. To update it from the host PC, the HSS console exposes the eMMC as a USB mass-storage device, after which a standard imaging tool writes the new image.

Procedure:

1. Connect the CAVU-HYPER-POLAR-DBG debug adapter and open the HSS console (Port 1 of the CP2105, 115 200 bps 8-N-1).
2. Connect a USB Mini-B cable from connector J4 on the debug adapter to the host PC. This exposes the PolarFire SoC native USB 2.0 interface.
3. Apply power (or assert reset). When the HSS countdown appears in the console, press any key to interrupt the boot sequence and drop to the HSS prompt.
4. At the HSS prompt, type `mmc` to select the eMMC interface, then `usbdmsc` to expose the selected eMMC as a USB mass-storage device.

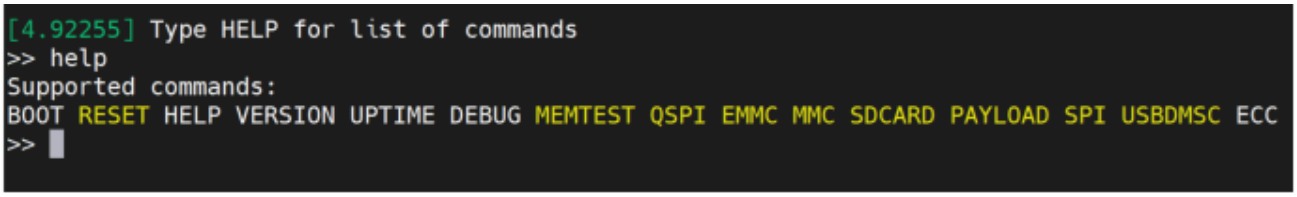

Figure 16: HSS Commands

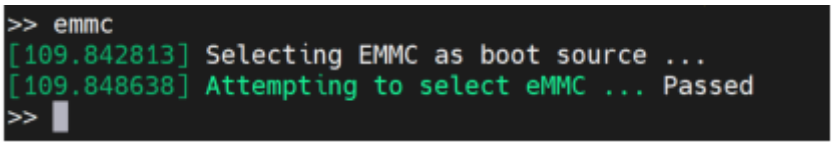

Figure 17: HSS emmc command

5. The host PC enumerates a new mass-storage device. Verify that the device size and identifier correspond to the OBC-HYPER-2 eMMC before any write operation.
6. Use Win32DiskImager, balenaEtcher, or `dd` to write the new Linux image (.img file) to the eMMC device.
7. When the write completes, eject the mass-storage device cleanly on the host PC. In the HSS console, press Ctrl+C to leave usbdmsc mode and return to the HSS prompt.
8. Type `boot` to launch the new image, or power-cycle the unit.

WARNING Verify the target device path (e.g. /dev/sdX on Linux, or the disk number on Windows) before writing. Writing to the wrong device will destroy data on that device.

5.4 Updating the FPGA Design and HSS

The PolarFire SoC fabric is non-volatile; updating the FPGA design means writing a new factory image into the device through JTAG. The HSS that lives in the device's eNVM is updated in the same JTAG transaction. No QSPI bitstream programming is required, because the fabric is not configured from QSPI at power-up.

Procedure:

1. Connect the CAVU-HYPER-POLAR-DBG debug adapter to the 15-pin JTAG/USB/Debug Micro-D connector on the back panel.
2. Connect a Microchip FlashPro5 or FlashPro6 programmer to the 10-pin 2×5 header on the debug adapter.
3. Launch Microchip FlashPro Express on the host PC and import the PolarFire SoC Job file (.job) supplied by CAVU. The .job file packages the fabric image plus the eNVM-resident HSS into a single atomic programming job.
4. Click Program. Programming takes several minutes. Do not remove power or unplug the FlashPro programmer during this operation.
5. Power-cycle the unit to boot with the new FPGA design and HSS.

CAUTION Interrupting the FlashPro programming operation may leave the device in an indeterminate state. Recovery is performed by re-running FlashPro Express with a valid .job file.

NOTE Customer fabric designs (Libero SoC projects) are integrated by CAVU and delivered as a signed .job file. CAVU does not publish raw bitstreams to end users.

5.5 Bare-Metal Software Development

Bare-metal applications can target either an individual U54 hart or the full MSS complex. The toolchain is Microchip SoftConsole v2022.2 or later, used with a FlashPro5/6 programmer for JTAG-based debug.

In the standard OBC-HYPER-2 delivery configuration, HSS remains resident in eNVM and acts as the first-stage boot supervisor. Customer bare-metal or RTOS applications are normally built as HSS payloads and loaded by HSS into the selected execution memory before the target U54 hart or harts are released.

Procedure:

1. Install Microchip SoftConsole and Libero SoC on the development host. Clone or import the desired bare-metal example from the Microchip PolarFire SoC bare-metal examples repository on GitLab.
2. Configure the project for the OBC-HYPER-2 target, using MPFS250T or MPFS460T as appropriate. Use the MSS configuration files supplied by CAVU with the .job file.
3. Connect the FlashPro5/6 programmer to the debug adapter. Build, load, and debug the application directly into LIM or DDR through SoftConsole during development.
4. For persistent boot execution, package the application as an HSS payload and store it in the configured non-volatile boot location used by the delivered boot chain.

Memory targets for bare-metal execution:

- LIM (Loosely Integrated Memory) — fast load, low latency, not persistent across reset. Recommended for iterative debug and time-critical routines.
- eNVM — reserved for HSS in the standard delivery configuration. Direct eNVM execution of a customer application is a special factory/development configuration and is not the normal customer application deployment path.
- DDR — largest available memory region. Recommended for larger bare-metal or RTOS applications loaded by HSS at boot.

> **NOTE** Regenerate the MSS configuration files in SoftConsole whenever CAVU delivers an updated .job file containing a new MSS configuration.

5.6 Network Configuration

All two Ethernet ports (LAN1, LAN2) are configured by default to obtain an IPv4 address by DHCP. After Linux boots, the standard tooling applies:

- `ip addr show` — list assigned addresses;
- `ssh` — secure-shell remote login;
- `scp` / `sftp` — secure file transfer;
- `nmcli` or edits to `/etc/network/interfaces` — static IP configuration.

5.7 Tool and Software Reference

Tool	Purpose	Version / source
FlashPro Express	PolarFire SoC fabric + eNVM (HSS) programming over JTAG	Microchip, latest
SoftConsole	Bare-metal C/C++ IDE with JTAG debug	Microchip, v2022.2 or later
Libero SoC	Full PolarFire SoC design suite (MSS configurator, fabric synthesis)	Microchip, v2022.2 or later
CP2105 USB VCP driver	Virtual COM-port driver for HSS / Linux console	Silicon Labs, latest
PuTTY / Tera Term / minicom	Serial terminal	Vendor's latest
Win32DiskImager / balenaEtcher / dd	eMMC image writing	Vendor's latest
HSS Payload Generator	Builds the signed payload blob loaded from QSPI/eMMC	Open-source, Microchip PolarFire SoC HSS repository

Table 28 — Tools & Software Reference

5.8 Watchdog and System Monitoring

The OBC-HYPER-2 implements an independent hardware watchdog and a layered software monitoring subsystem. The watchdog and the on-board health-monitoring telemetry are described in a dedicated document, supplied separately:

CAVU-OBC-HYPER-POLAR-WDM_v1.0 — Watchdog and System Monitoring Description.

That document covers watchdog architecture (window timing, kick protocol, reset propagation), the per-hart software heartbeat managed by HSS on the E51 monitor core, FDIR thresholds, and the housekeeping telemetry exposed to the spacecraft. It is referenced here only by name; the present user manual does not duplicate its content.